

DIFFERENTIAL NON-LINEARITY CORRECTION FOR SUCCESSIVE APPROXIMATION ADC

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Abstract: In this paper a new method to correct the differential non-linearity(DNL) error for a successive approximation is proposed. The DNL of ADC is very important characteristic in the field of radiation pulse height analysis or measurement of probability density function. The results of computer simulations are shown to demonstrate the feasibility of the proposed correction method.

1.Introduction

The ADC which is used in a multichannel pulse height analyzer(PHA) or a measuring instrument of probability density function must have excellent differential linearity. Because of its good differential linearity and simple circuit, the Wilkinson type is still extensively used as an ADC for pulse height analyzers, but it has comparatively long conversion time. The successive approximation type ADC has quite short conversion time and is easy to get, but has very wrong differential linearity. The "Sliding Scale Method" by Gatti was introduced about 25 years ago to compensate the channel width inaccuracies of successive approximation ADC. The aim of this paper is to propose a new method to correct the DNL error of amplitude distribution curve which is measured by successive approximation ADC.

2. DNL analysis of successive approximation ADC

Block diagram of successive approximation ADC is shown in Fig.1. It is clear that the largest cause for the DNL error of successive approximation ADC is the differential linearity of D/A converter (DAC) in it. The basic ADC circuit (ladder resistor network) is shown in Fig.2. where, I_0 : Constant current, G : Conductance, I_1 - I_8 : 2^n weighted current, n : nodes for circuit analysis. For the ladder resistor network in Fig.2, we can get the circuit equation in the form of a matrix equation (1). Where, i_1 - i_8 are the current flowing into the nodes n_1 - n_8 respectively. and v_1 - v_8 are node voltages respectively. $i_1=I_0, i_2=i_3=\dots=i_8=0$

Solving the equation (1) with respect to v_1 - v_8 , we get the output current of DAC. Since the registers which are used in the DAC are not ideal, the output current of DAC is not also ideal. Moreover, it is impossible to obtain the ideal semiconductor switch.

The differential linearity error of DAC is the amount of deviation of any quantum from its ideal value. In other words, it is the deviation in the analog difference between two adjacent codes from the ideal value of Full scale range/ 2^n .

The output current is explained as follows,

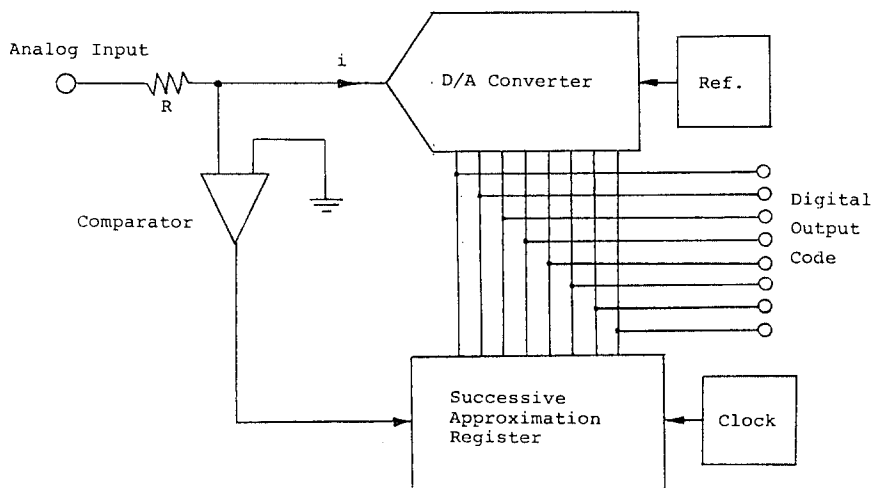


Fig.1 Block diagram of successive approximation ADC.

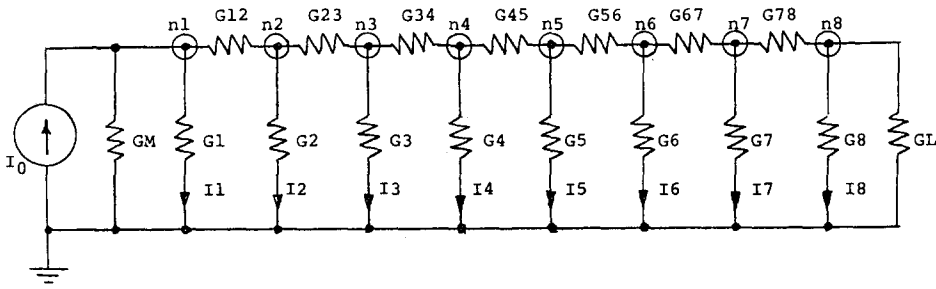


Fig.2 Ladder resistor network.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \\ i_7 \\ i_8 \end{bmatrix} = \begin{bmatrix} g_1 & -G_{12} & 0 & 0 & 0 & 0 & 0 & 0 \\ -G_{12} & g_2 & -G_{23} & 0 & 0 & 0 & 0 & 0 \\ 0 & -G_{23} & g_3 & -G_{34} & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_{34} & g_4 & -G_{45} & 0 & 0 & 0 \\ 0 & 0 & 0 & -G_{45} & g_5 & -G_{56} & 0 & 0 \\ 0 & 0 & 0 & 0 & -G_{56} & g_6 & -G_{67} & 0 \\ 0 & 0 & 0 & 0 & 0 & -G_{67} & g_7 & -G_{78} \\ 0 & 0 & 0 & 0 & 0 & 0 & -G_{78} & g_8 \end{bmatrix} \times \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \\ v_7 \\ v_8 \end{bmatrix} \quad (1)$$

$$\begin{array}{ll}
 g_1 = G_{11} + G_1 + G_{12} & g_5 = G_{45} + G_5 + G_{56} \\
 g_2 = G_{12} + G_2 + G_{23} & g_6 = G_{56} + G_6 + G_{67} \\
 g_3 = G_{23} + G_3 + G_{34} & g_7 = G_{67} + G_7 + G_{78} \\
 g_4 = G_{34} + G_4 + G_{45} & g_8 = G_{78} + G_8 + G_L
 \end{array}$$

$$\begin{aligned}
 I_{out} &= s_1 G_1 v_1 + s_2 G_2 v_2 + \dots + s_8 G_8 v_8 \\
 &= s_1 I_1 + s_2 I_2 + \dots + s_8 I_8 \quad (2)
 \end{aligned}$$

Where, $s_1 - s_8$ are the DAC input code 0 or 1.

The channel width ΔV_k are proportional to the output current k difference of DAC.

$$\Delta V_k \propto (I_{out,k+1} - I_{out,k}) \quad (3)$$

The differential non-linearity error DNL is defined as

$$E_{DNL} \triangleq \frac{\max. [\det. (\Delta V_k - \overline{\Delta V})]}{\overline{\Delta V}} \times 100 [\%] \quad (4)$$

Where, $\max. [\cdot]$ gives maximum value
 $\det. (\cdot)$ gives absolute value
 $\overline{\Delta V}$ is average of ΔV_k

Fig.3 shows the channel width excursions from the ideal when one of resistor deviates 1[%] from the ideal. The MSB resistor generates the biggest DNL. The LSB resistor generates small but many DNL.

3. Establishment of algorithm for DNL error correction

Investigating the characteristics of DAC in Fig.3, we can assume that the S channels increase α [%] ($\alpha \geq 0$) and the remaining N-S channels decrease β [%] ($\beta \geq 0$) when just one resistor deviates independently from the ideal. Then we obtain the equation,

$$\overline{\Delta V} \times \frac{\alpha}{100} \times S = \overline{\Delta V} \times \frac{\beta}{100} \times (N-S) \quad (5)$$

This reduces to,

$$\alpha S = \beta (N-S) \quad (6)$$

More over, we obtain,

$$\sum_{i=1}^S \frac{C_{s,i}}{1 + \frac{\alpha}{100}} + \sum_{j=1}^{N-S} \frac{C_{r,j}}{1 - \frac{\beta}{100}} = \sum_{i=1}^S C_{s,i} + \sum_{j=1}^{N-S} C_{r,j} \quad (7)$$

Where, $C_{s,i}$ ($i=1,2,\dots,S$) are the counting data of increased channel width. $C_{r,j}$ ($j=1,2,\dots,N-S$) are the counting data of decreased channel width. That is to say, the sum of compensated counting number is equal to the total non-compensated counting number.

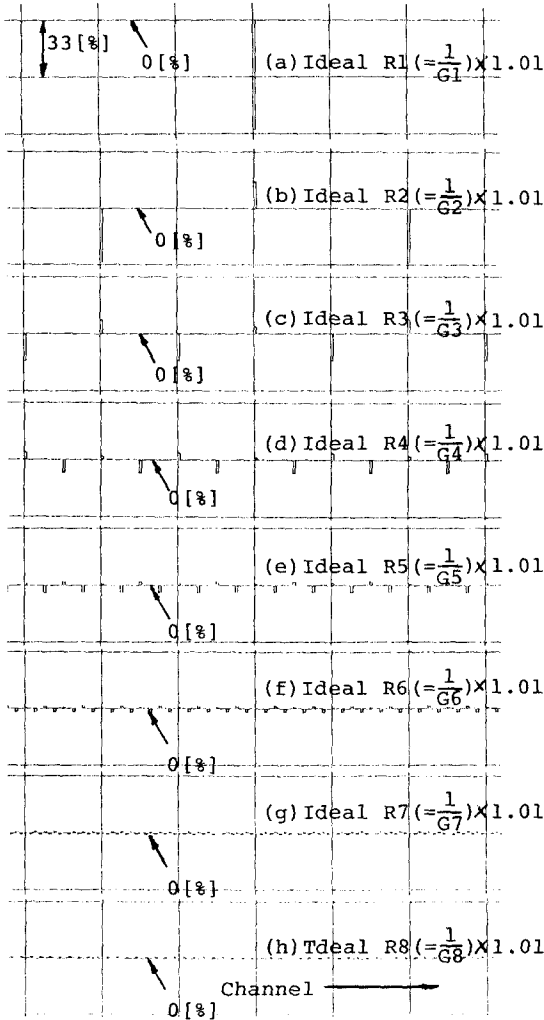


Fig.3 Excursions of V_k from the ideal when just one resistor deviates independently from the ideal.

We now solve equation (6) and (7) for the correction coefficients α and β . We thus obtain,

$$A = \left[X \cdot \frac{N-S}{S} - Y \right] / (X+Y) \quad (8)$$

$$B = \left[X - Y \cdot \frac{S}{N-S} \right] / (X+Y) \quad (9)$$

Where, $A \triangleq \frac{\alpha}{100}$ (10)

$$B \triangleq \frac{\beta}{100} \quad (11)$$

$$X \triangleq \sum_{i=1}^S C_{s,i} \quad (12)$$

$$Y \triangleq \sum_{j=1}^{N-S} C_{r,j} \quad (13)$$

Employing the solution A and B, we can establish the following algorithm in the form of a flowchart in fig.4.

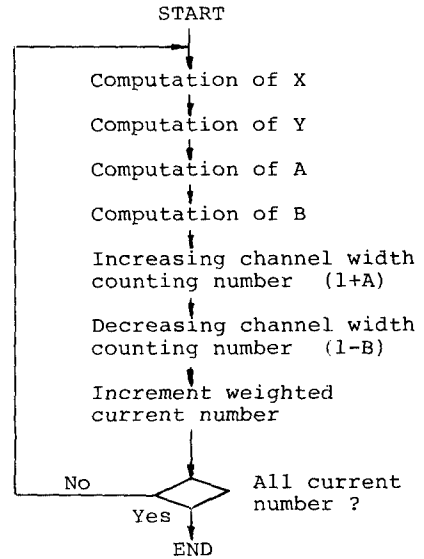


Fig.4 Flowchart for the proposed DNL error correction algorithm.

First, we compute the sum X and Y. And next, we compute A and B using X and Y. Then we multiply (1+A) to all channels of which the channel width is increased. And next, we multiply (1-B) to all channels of which the channel width is decreased. We repeat this procedure for all weighted current number. If necessary, whole procedure is repeated.

4. Computer simulations

On the assumption that a Gaussian distributed random pulses are exist in the background pulses, the computer simulations are carried out. A personal computer and the BASIC language are used. The results are shown in Fig.7 and Fig.8. As we can see in Fig.8, very small standard deviation is used for the signal. Nevertheless, the DNL error is well corrected. It is evident that if we use some smoothing technique to reduce the DNL error, for example "the moving average", the signal will surely destroyed.

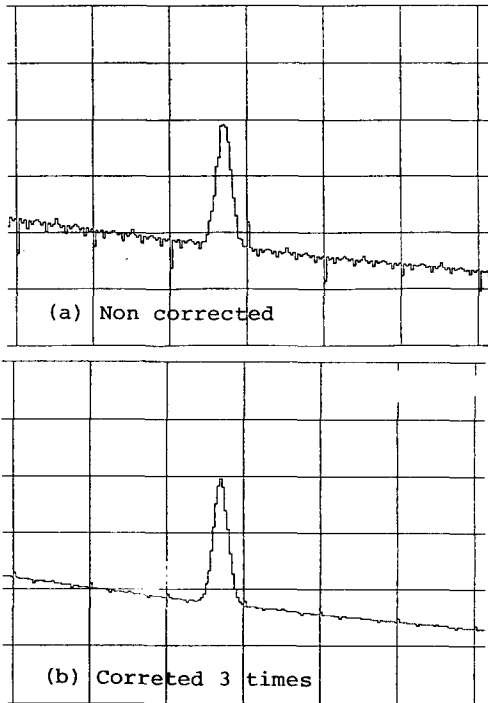


Fig.7 Computer simulation for a Gaussian random signal.

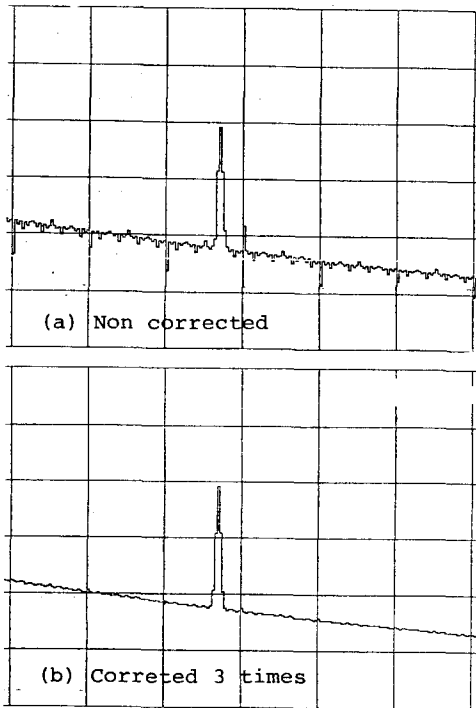


Fig.8 Computer simulation for a Gaussian signal with small standard deviation.

5. Conclusions

A new algorithm to correct the DNL of the successive approximation ADC is proposed in this paper. The remarkable feature of this method is that the effect of DNL error correction is independent of temperature. This method does not disturb the fastness and the dynamic range of the successive approximation ADC.

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