EPD time delay in etching of stack down WSix gate in DPS+ poly chamber

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Abstract

Device makers want to make higher density chips as devices shrink, especially WSix poly stack down is one of the key issues. However, EPD (End Point Detection) time delay was happened in DPS+ poly chamber which is a barrier to achieve device shrink because EPD time delay killed test pattern and next generation device.

To investigate the EPD time delay, a test was done with patterned wafers. This experimental was carried out combined with OES(Optical Emission Spectroscopy) and SEM (Scanning Electron Microscopy). OES was used to find corrected wavelength in WSix stack down gate etching. SEM was used to confirm WSix gate profile and gate oxide damage.

Through the experiment, a new wavelength (252nm) line of plasma is selected for DPS+ chamber to call correct EPD in WSix stack down gate etching for current device and next generation device.

1. Introduction

3 kinds of WSix gate structures were prepared to develop next generation device. The 1st device structure is 80nm SiON/180nm SiN/**100nm WSix/100nm poly**/4.5nm gate oxide. The 2nd device is 80nm SiON/180nm SiN/**120nm WSix/100nm poly**/4.5nm gate oxide. The 3rd device is 80nm SiON/180nm SiN/**100nm WSix/80nm poly**/4.5nm gate oxide. Fig.1 showed the trend of EPD time delay and device structure. The 1st device structure showed very stable EPD time from 1st wafer to last wafer. There was no yield loss and damage in this structure. The 2nd device structure showed a little unstable EPD time delay from 1st wafer to 4th wafer, but there was not any effect to device yield. The 3rd device structure showed very unstable EPD time delay and pitting on gate oxide through SEM. In this case, all wafers were killed due to gate oxide pitting.

For last one and half year we couldn't develop WSix gate stack down process using DPS+ chamber due to EPD time delay. Our final target structure is 80nm SiON/180nm SiN/**100nm WSix/45nm poly**/4.5nm gate oxide. In order to avoid WSix gate oxide pitting in **100nm WSix/80nm poly** structure, high selectivity WSix to poly process and low micro-loading process were tried. But both process development were failed in DPS+ poly chamber. EPD time delay, low selectivity WSix to poly and high micro-loading effect make gate oxide pitting and killed device, which is a barrier to go to next generation device process development using DPS+ poly chamber.

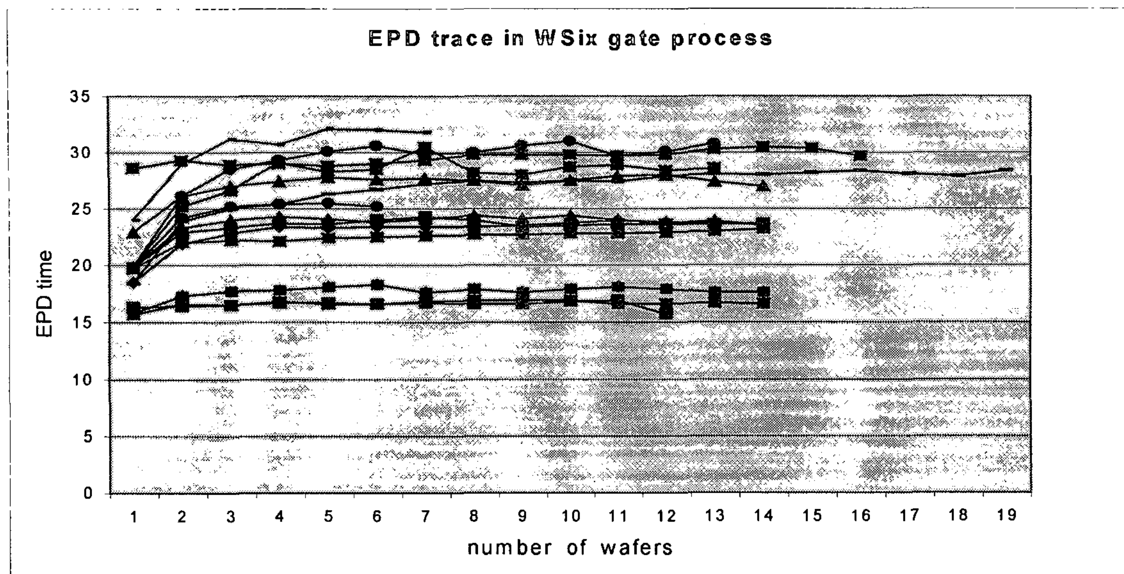

Fig.1 EPD trace and device structure in WSix gate etching

2. Experimental

OES system is installed in DPS+ chamber which has scan spectrometer to analyze corrected wavelength of plasma. Scan spectrometer can analyze correct wavelength from 200 to 800nm during plasma on. EPD wavelength (281nm) was confirmed through scan spectrometer. SEM is used to see etching profile and gate oxide damage. After SEM result is O.K, test was done with real wafers.

3. Result

◎ Applied new chamber seasoning

chamber seasoning A (Deposition mode)
ME : SF_6/Cl_2, a_1 mTorr, a_2 Ws, a_3 Wb, a_4 sec
OE : HBr/O_2, b_1 mTorr, b_2 Ws, b_3 Wb, b_4 sec

The above condition was polymer deposition mode during chamber seasoning. So clean mode condition is applied as new chamber seasoning. Fig.2 showed EPD trend within cassette depending on chamber seasoning.

new chamber seasoning (Clean mode)
ME : SF_6/Cl_2, a_1 mTorr, a_2 Ws, a_3 Wb, c_1 sec
OE : HBr/O_2, b_1 mTorr, b_2 Ws, b_3 Wb, d_1 sec

According to test result, no chamber seasoning (much polymer deposition mode) and 5 wafers chamber seasoning (much clean mode) condition were affected to EPD time delay. 2 wafers chamber seasoning reduced 50% EPD time delay. So proper seasoning reduced EPD time delay.

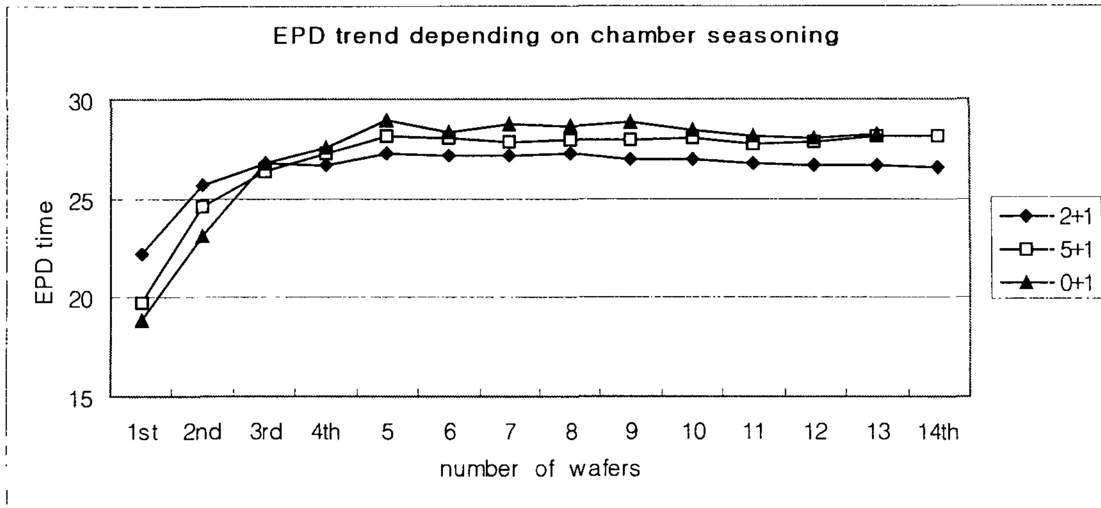

Fig.2 EPD trend within cassette depending on chamber seasoning.

- Extended AGC time

There are many parameters in EPD main menu to call correct endpoint time. AGC (Auto Gain Control) time is one of the parameters. If this parameter is too short or not proper, EPD trace is not stable or repeatable. We used 5sec in AGC, which is not proper to call EPD time at next generation device. So extended AGC time from 5sec to 10sec was tested with test wafers. Etch profile and gate oxide damage were confirmed by SEM. Fig.3 showed WSix gate etching profile and no oxide damage. Real production wafers were processed with 10sec in AGC. Fig.4 showed stable EPD trace and decreased EPD time delay by 50%. So extended AGC time reduced EPD time delay.

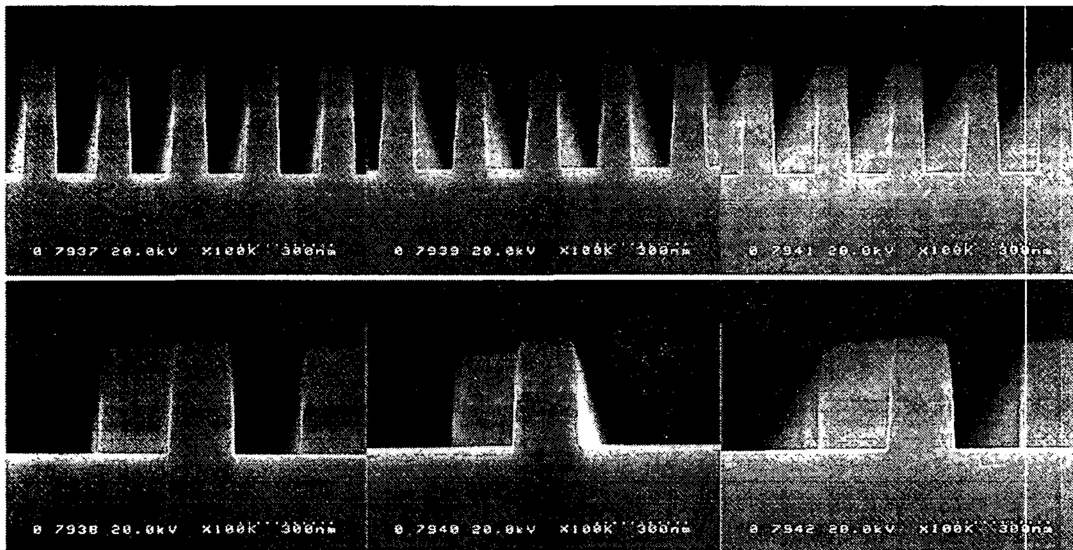

Fig.3 WSix gate etching profile after applied extended AGC time

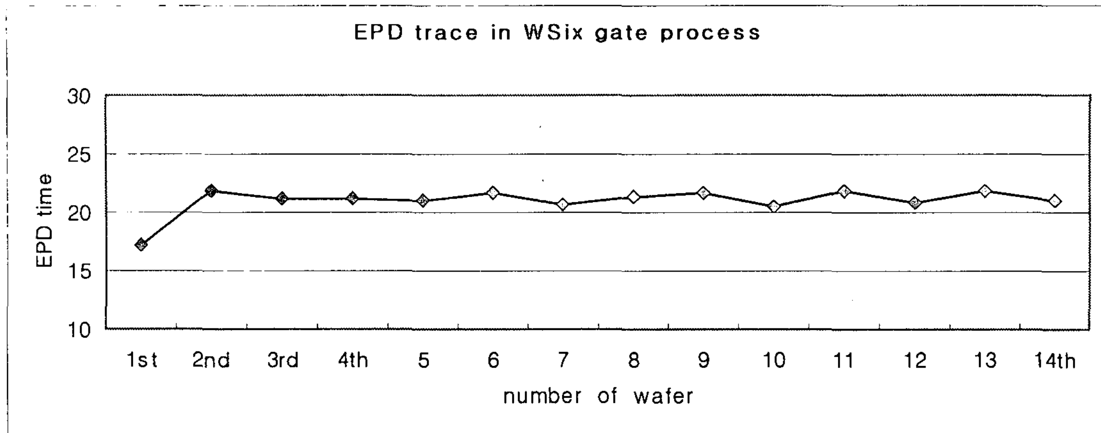

Fig.4 EPD time delay is decreased by 50% after applied extended AGC time

◎ Found new wavelength

We tried 281nm line to call EPD which is actually unknown wavelength in the etching system. To confirm this wavelength, scan spectrometer was adapted to find correct wavelength in WSix gate etching. It showed several wavelength during etching of WSix and poly film respectively. Fig.5 showed several lines such as 281nm, 288nm, 252nm, 439nm, 453nm in WSix film etching.

Fig.6 showed 252nm, 281nm, 288nm, 439nm, 453nm lines in poly film etching. 252nm line had high plasma intensity in WSix film etching and 252nm line showed very low plasma intensity as poly film etching. 252nm line showed the high gap of plasma intensity between WSix and poly film etching. So 252nm line was selected to call correct EPD.

Fig.7 showed etch profile and no gate oxide damage. Real production wafers of next generation device were processed with 252nm wavelength. Fig.8 showed no EPD time delay and a good reliability. So new wavelength (252nm) line makes clear and removes EPD time delay within cassette.

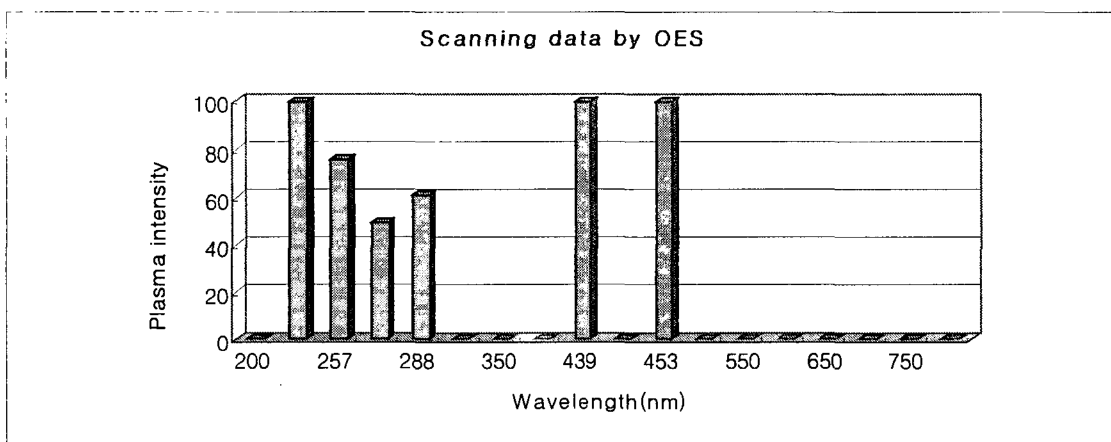

Fig.5 New wavelength in WSix gate film etching through plasma scan

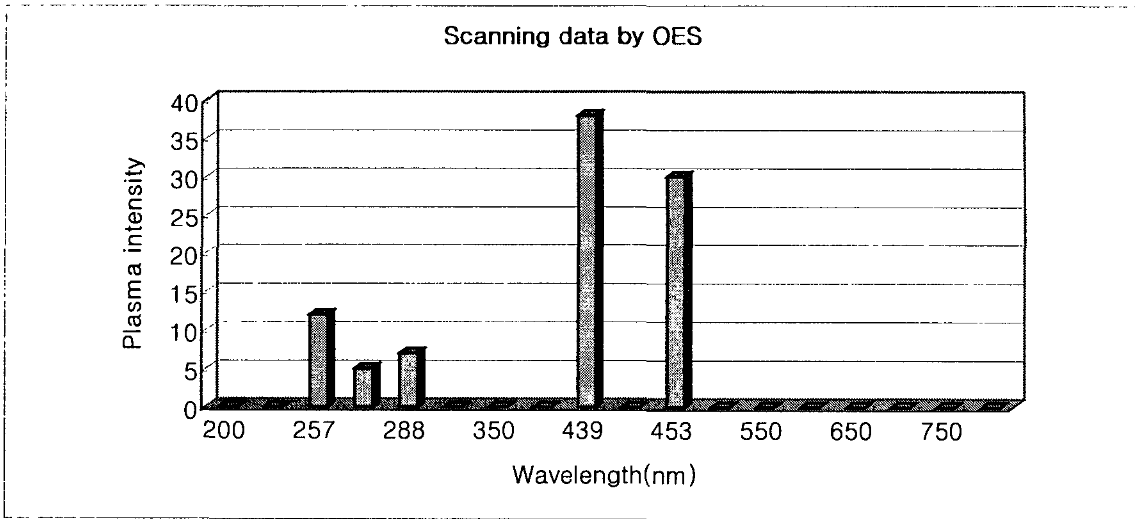

Fig 6 New wavelength in poly film etching through plasma scan

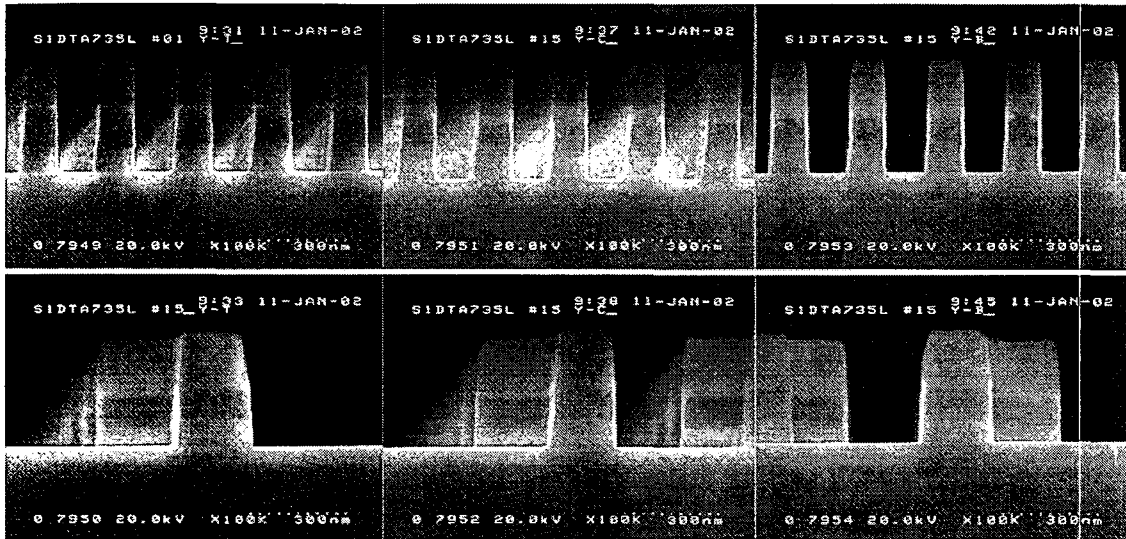

Fig.7 WSix gate etching profile after applied extended new wavelength 252nm

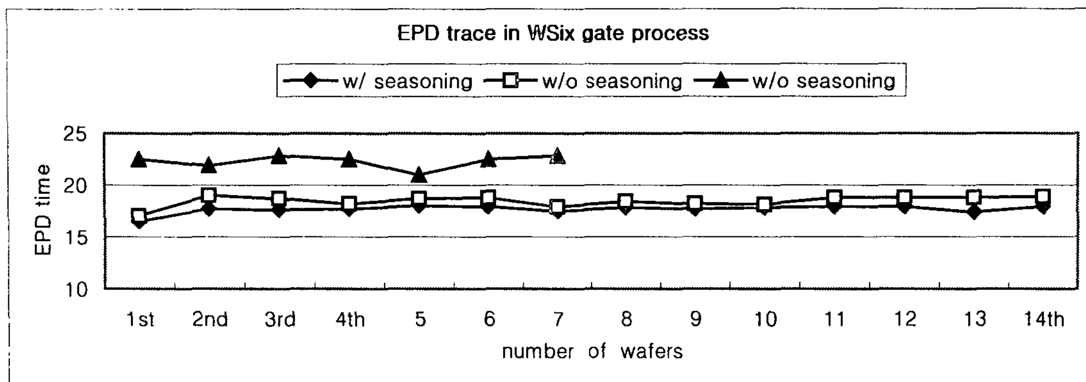

Fig.8 EPD time delay is disappeared after applied new wavelength 252nm line

According to our test result, 3 kinds of solution were found to clear EPD time delay. Proper clean mode chamber seasoning was better than deposition mode during chamber seasoning. So clean mode chamber seasoning was selected to reduce EPD time delay. Extended AGC time in EPD main menu showed good performance and repeatability. So 10sec AGC time is selected to reduce EPD time delay in EPD main menu.

New wavelength 252nm was selected through plasma scan, which showed high plasma intensity gap during WSix and poly film etching respectively. 252nm line has a good repeatability and no EPD time delay. So this 252nm line was selected to run not only current device structure but also next generation device without EPD time delay. Customer was satisfied with the above test items and results on EPD time delay.

Fig.9 showed the trend of EPD time delay and device structure after applied new chamber seasoning, Extended AGC time and new wavelength(252nm). Even though EPD time delay was cleared through test, WSix gate etching has some process issue, which are low selectivity and high micro-loading effect in DPS+ chamber. So far customer request high selectivity and low micro-loading effect in WSix gate poly etching.

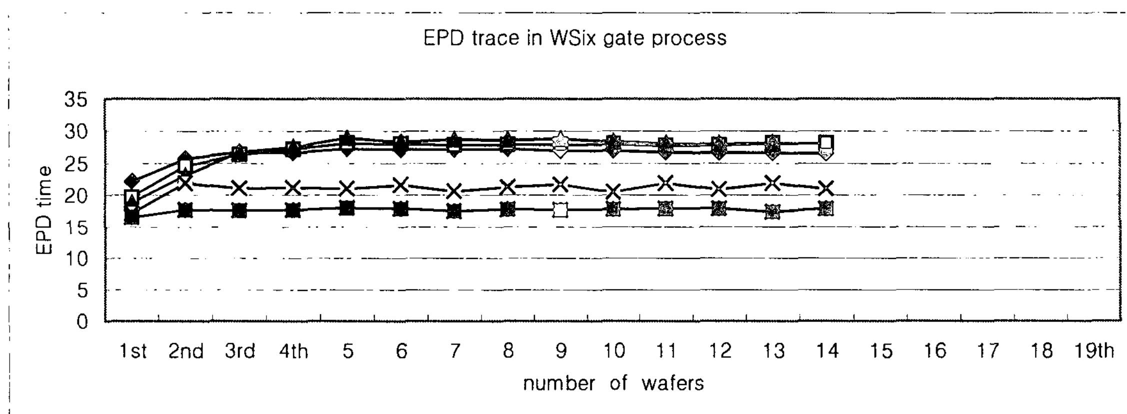

Fig.9 EPD trace after applied new wavelength depending on device structure

4. Future direction

As devices shrink, Device makers request a very high system hardware performance and a critical process specification. Base on these requirements, the DPS II system is developed system hardware and process. A new process was developed with a specification and it showed high performance such a high selectivity WSix to poly and a low micro-loading effect. DPS II can install 2 types endpoint system to get corrected endpoint time. One is OES and the other is IEP (Infrared End Point). If 2 endpoint systems are combined in DPS II poly chamber, there is no EPD time delay any more.

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