초청강연

플렉서블 디스플레이 기술동향 및 전망

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Flexible Display 기술 동향 및 전망

2004. 6. 3.

김 보 성

차세대 Display팀
삼성전자

FPD Technology Mega Trend

FPD Panel은 TFT-LCD를 “기본축”으로 고성능·저가격화, 복합화로 발전

Active-OLED (LTPS-Base)  Sheet Computer (SoC)

TFT-LCD (LTPS)  

TFT-LCD (a-Si)  극저전기 초대형 LCD-TV

Color STN  Flexible FPD

B/W TN  Passive-OLED (STN-Base)

Passive-Matrix  Active-Matrix

Now
Display Technology Tree

Electronic Displays

Display Mode

- CRT
- LCD
- PDP
- EL

Driving Mode

- Active
  - a-Si TFT
  - LTPS
  - Organic TFT
- Passive

Flat Panel Display

- e-Paper

Flexible Display Is...

Display Free from Form Factors (Glass ➔ Plastics)

➤ Creating New Market beyond Conventional FPD Application

Advantages

- More rugged
- Lighter weight
- Foldable
- Conformal
- Flexible
- Roll-to-roll compatible
- Very low cost
## Key Technology for Flexible Displays

<table>
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<th>Issues</th>
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<tr>
<td>Materials</td>
<td>• Substrate handling of flexible plastic film</td>
</tr>
<tr>
<td></td>
<td>• Gas barrier</td>
</tr>
<tr>
<td></td>
<td>• Soluble insulator, semiconductor, and conductor</td>
</tr>
<tr>
<td>Equipment</td>
<td>• Low temp. &amp; low pressure deposition</td>
</tr>
<tr>
<td></td>
<td>• Printing (inkjet, micro-contact, soft-lithography..)</td>
</tr>
<tr>
<td></td>
<td>• Roll to roll type equipment</td>
</tr>
<tr>
<td>Process</td>
<td>• CTE mismatch of layers</td>
</tr>
<tr>
<td></td>
<td>• Film stress management</td>
</tr>
<tr>
<td></td>
<td>• Low temperature process</td>
</tr>
<tr>
<td>Display mode</td>
<td>• OLED, LCD, e-Ink, other new display mode..</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>• Module containing driver bonding</td>
</tr>
<tr>
<td></td>
<td>• Product's stability and reliability</td>
</tr>
</tbody>
</table>

## Flexible Display 개발 현황

<table>
<thead>
<tr>
<th>Maker</th>
<th>E-ink</th>
<th>Sony</th>
<th>SEIKO EPSON</th>
<th>Tokyo Univ.</th>
<th>Sharp</th>
<th>Stuttgart Univ.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub.</td>
<td>250 um SUS (transfer) Plastic (transfer) Plastic (FLC) Plastic PI</td>
<td>100 um PES</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fig.</td>
<td><img src="image" alt="E-ink" /></td>
<td><img src="image" alt="Sony" /></td>
<td><img src="image" alt="SEIKO EPSON" /></td>
<td><img src="image" alt="Tokyo Univ." /></td>
<td><img src="image" alt="Sharp" /></td>
<td><img src="image" alt="Stuttgart Univ." /></td>
</tr>
<tr>
<td>Ref.</td>
<td>Y. Chen E Ink Corp. SID 01 p 157 (2001)</td>
<td>A. Asano, Sony, Japan SID 03</td>
<td>S. Utsumo, SEIKO EPSON, IDW 01</td>
<td>H. Inajikake, Tokyo Univ. Japan, IDW 03</td>
<td>Sharp, Japan SID 02</td>
<td>M. Muecke et. al. Stuttgart, Germany</td>
</tr>
</tbody>
</table>
Electrophoretic Display by e-Ink

2” Flexible a-Si TFT e-Ink (SID Digest 2001.157.; e-Ink)

Figure 7. A display bent to a radius of curvature of 2 inch
- Polyester/ITO sheet thickness : 125 um
- Steel Foil thickness : 250 um
- Display total thickness : 475 um
- Pixels : 52x64
- Size : 1.3 inch x 1.6 inch
- Aperture Ratio : 70%

Figure 6. Display image, demonstrating the wide viewing angle of the display.

Electrophoretic Display by e-Ink

3” a-Si TFT e-Ink; E Ink
(Nature 2003, 423, 136.)
- Resolution : 160 X 240 (96ppi)
- White reflectance : 43%
- Contrast 8.5:1
- 75um Steel-foil Substrate
Reflective Plastic LTPS TFT-LCD

3.8" Flexible LTPS TFT-LCD *(SID Digest 2003.988.; Sony)*

- PDA size of 3.8 inch (diagonal)
- panel thickness ~ 0.4 mm
- weighs ~ 3 grams
- 320 x RGB x 240 : 230,400 dots

TFT Transfer Process by Sony
A flexible LTPS TFT on a 300mm x 350mm and a 0.2-mm-thick plastic substrate with nine dies for 3.8-inch-diagonal size LCDs.

Flexible LTPS TFT-LCD

8.4” Flexible LTPS TFT-LCD

(IDW 2002.319.; Toshiba)

- Resolution: 119ppi (800 X 600)
- Contrast > 200:1
- Slim Glass
- Column Spacer
- Curvature radius : 200 mm
- Drive IC Built-in Type
- Panel Thickness : 0.4 mm
- Weight : 20g

The array glass substrate was thinned to several tense microns from the back of the substrate by the newly developed methods, and then attached to flexible substrate
Plastic a-Si TFT-LCD

4" Plastic a-Si TFT-LCD  
*(SID Digest 2002, 1204.; Sharp)*

- Resolution : 240 X 240 (85ppi)  
- Aperture Ratio : 92%  
- Pixel Size : 100 X 300 um  
- Low CTE Plastic Substrate

0.2mm novel plastic substrate의 양면에 base coating (the sputter-deposited SiNx)  
Gate electrode formation at room temp.  
SiNx, a-Si:H, n+ a-Si:H deposition(350/150/50nm) by PECVD at 220℃  
active → S/D → n+ a-Si dry etching

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Plastic a-Si TFT-LCD

(a) The conventional plastic substrate  
(b) The novel plastic substrate  
Figure 4. Curvature of plastic substrates deposited PECVD films

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220도에서 thermal damage가 없는 plastic으로 mobility 0.3cm2/V.s, Vth 2.0V, Ioff <1pA, On/Off ratio ~6 (gate -10~+15V) 얻음
Plastic AM-OLED

2.1” Plastic AM-OLED (SID Digest 2003, 865.; Seiko Epson)

- Resolution : 200 X 150 (120ppi)
- Scanning Driver : 5.0 kHz, 6-8V
- Signal Driver : 333kHz, 6-8V
- EL, Ink-jet Printing
- Thickness 0.7mm
- Weight : 3.2g

Transfer Mechanism in Surface Free Technology by Laser Annealing / Ablation (SUFTLA®)
Organic TFT

6” OTFT e-Ink; Lucent
2.1” OTFT PDLC; Philips

- Number of Lines: 16 X 16
- Pixel Size: 1cm X 1cm
- TFT Size: 1mm

- Number of Lines: 96 X 64
- Polythiophenevinylene
- Mobility: 0.001cm²/Vs
- I_on/off = 10³

Flexible OTFT e-Ink

2” OTFT e-Ink; Philips (Nature Materials 2004, 1.)

- Number of Lines: 64 X 64
- Pixel Size: 540X549 um
- Curvature Radius: 1 cm
- Soluble Pentacene

25-um-thick polyimide foil laminated on a removable Si support wafer of 150 mm diameter.
The gate dielectric was a 350-nm-thick photoimageable polyvinylpheno.
100-nm-thick precursor pentacene film was spincoated.
Flexible OTFT e-Ink

4.7" OTFT e-Ink; PolymerVision
(IDW 2003, 1663.)

- Resolution: 85ppi (320 X 240)
- Pixel Size: 300X300 um
- Aperture Ratio: 77%
- Thickness: 300 um
- Curvature Radius: 2 cm
- Mobility: 0.02 cm2/Vs
- W/L: 140/5
- Soluble Pentacnene

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Electrophoretic Display의 원리

Top transparent electrode
Clear Fluid
Positively charged white pigment chip
Negatively charged black pigment chips
Bottom electrode

Subcapsule addressing enables high-resolution display capability

Light State

Black & White Mode

E-Ink Display Structure

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- PET
- ITO
- Ink Layer
- Adhesive
- Polarizer
- Color Filter
- Color Filter Glass
- Liquid Crystal
- TFT Glass
- Polarizer
- BackLight
- E-Ink Frontplane
- Plastic Film
- Laminator
- 0.1 mm
Electrophoretic Display의 장점

- long-term image stability
- extremely low power consumption
- high white state reflectivity and contrast
- paper-like optics for enhanced readability and legibility
- full view angle
- AMLCD에 비해 보다 경고하고 단순한 assembly process

5.7" a-Si TFT e-Ink Module

- Resolution : hVGA (480*320 line)
- Reflectance : 40.0% (White)/4.7% (Black)
- Contrast Ratio : 8.5
Plastic a-Si TFT-LCD
Using Low Temp. Process

Technical Challenges

- **a-Si TFT process**
  - Direct process on plastics
  - Low temp. (< 150°C CVD) process
  - Film stress management
  - Layer to layer alignment

- **Color filter on plastics**
  - Low temp. process
  - New color PR

- **LC Assembly process**
  - New materials (spacer, sealant)
  - Assembly with fine alignment

- **Flexible backlight**
  - Film-type Inorganic EL
Plastic a-Si TFT Array Structure

Gate Dielectrics
(organic/inorganic)

Film Stress Management

• Gate Insulator

Only Inorganic
Active layer

Organic + thin Inorganic
Active layer

Strain : 0.18%

4.5 cm

Strain : 0.095%

1 cm
Isolation of Active Area

❖ Stress by the Difference of CTE

- Inorganic layer (CTE: 5 ppm/K)
- Plastic (CTE: 52 ppm/K)
- 150 °C
- Due to difference of CTE
- Elongation, stress
- Released stress by patterning inorganic layers

Shape of TFT array on plastic after deposition of active layers

Shape of TFT array on plastic after patterning of inorganic layers

Layer to layer alignment

❖ Due to CTE Mismatch between plastic substrate and thin films

- Thermal annealing of substrate
- Substrate barrier coating
- TFT array design compensating misalignment
TFT Performance

 Thermal annealing effect:

- The on current was increased to $\sim 10^{-6}$ A and Vth was decreased to 5.34 V after annealing the TFT array.
- The off current was below $10^{-12}$ A.
- The on/off ratio was more than 6 decades (@ Vg = -7V ~ +20V)

Low Temperature Color Filter Process

 Low temp. curable color PR

- Low temperature-curable color PR applied with new thermal polymerization system: cure temp. 150 °C
- Color difference after chemical test (NMP, γ BL, NaOH, Acetone, IPA) : $\Delta E_{ab} < 5$
- Color reproducibility : 30%
Plastic 2.2” a-Si:H TFT-LCD Sample

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Panel Size</td>
<td>2.2 inch</td>
</tr>
<tr>
<td>Resolution</td>
<td>128 X 160 X 3 (93dpi)</td>
</tr>
<tr>
<td>Aperture Ratio</td>
<td>46%</td>
</tr>
<tr>
<td>Color Gamut</td>
<td>30%</td>
</tr>
<tr>
<td>Transmittance</td>
<td>7.8%</td>
</tr>
<tr>
<td>Luminance</td>
<td>55 cd/m²</td>
</tr>
<tr>
<td>Panel Thickness</td>
<td>0.82 mm</td>
</tr>
<tr>
<td>Panel Weight</td>
<td>2.9 g</td>
</tr>
<tr>
<td>Module Thickness</td>
<td>1.2 mm</td>
</tr>
<tr>
<td>Module Weight</td>
<td>4.4 g</td>
</tr>
<tr>
<td>Substrate</td>
<td>PES</td>
</tr>
</tbody>
</table>

TFT Array on Plastics
Using Organic Semiconductor

- 26 -
Field Effect Mobility of OTFT

OTFT Main Issues

What can be the main issues in OTFT Device to make “Paper-like Price Flexible Display”? 

1. **Organic Semiconductor Formation**: Evaporation or Printing? 
2. **Gate Insulator**: Inorganic or Organic? 
3. **Interface Handling**: Organic Semiconductor / Insulator 
4. **Sid contacts**: What is best material? 
5. **Patterning**: Photolithography, Shadow Mask or Printing? 
6. **TFT Structure & Performance Improvement**: What is optimum structure? 
7. **TFT Stabilities**: What is best passivation material? 
8. **Array Structure**: What is optimum architecture? 
9. **Plastic Substrate**: Performance or Cost?
Pentacene Based High-Performance OTFT Review

Penn State Univ. (T. N. Jackson et. al, DRC Conf. Dig., 1999)
- Using thermally grown SiO₂ as an insulator (Top contact)
- Modification of dielectrics using OTS
- Mobility : 2.1 cm²/Vs

Infineon (H. Klauck et. al, J. Appl. Phys., 2002)
- Using cross-linked polyvinylphenol (PVP) as a gate insulator (Top contact)
- Mobility : 3.0 cm²/Vs, Vth = -5 V, Ion/off = ~10⁶

- Using alumina as a gate insulator (Top contact)
- Modification of dielectrics using alkylphosphonic acid monolayer
- Mobility : 0.1 ~ 3.3 cm²/Vs, Ion/off = ~10⁶

OTFT Structure Issues for Array Fabrication

Top Contact
- Better in TFT Property
  ⇒ Easy to control the channel interface
- Need thermal evaporation using shadow mask for S/D patterning
  ⇒ Difficult to control channel length

  • Impossible to make high resolution OTFT array
    (min. resolution : ~ 40 μm)

  • For the high resolution OTFT array, need to develop
    New organic semiconductor material with high chemical & moisture resistance
    OR
    New TFT Architecture
OTFT Structure Issues for Array Fabrication

Bottom Contact

- Possible to make High Resolution Array
  ⇒ Easy to have the channel length shorter by photolithography for S/D
- Lower TFT Performance
  ⇒ Hard to maintain good interface condition on organic insulator

- Interface treatment
- Stability & resistance of an organic gate insulator during TFT processes are key issues for bottom contact TFT structure

- For improving & stabilizing “bottom contact OTFT” performance, need to develop New Organic Gate Insulator material with high chemical resistance

OTFT Unit Device Performance

☐ Required Properties for Gate Insulators
  ▶ Low Leakage Current
  ▶ Low Surface Roughness
  ▶ High Stability against Moisture & Oxygen
  ▶ High Resistance for Chemical & Solvent
  ▶ Higher K
  ▶ Low Charge Trapping Center

S
D
 Au (W/L = 1000/100um)
OSC (pentacene)
Insulator (S1 & 2)
Gate Electrode (Al/Nd)
Substrate (Glass)

[TFT Device]
## Development of New Organic Gate Insulator: S1

- Wet processible organic gate insulator
- Derivative of Polyvinylphenol (PVP)
- New material designed and synthesized by SAIT

<table>
<thead>
<tr>
<th>Dielectrics</th>
<th>Mobility * (cm²/Vs)</th>
<th>On/Off Ratio</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>4~6</td>
<td>~ 10⁶</td>
<td>Samsung (2003)</td>
</tr>
<tr>
<td>Polyimide</td>
<td>0.2</td>
<td>10³ ~ 10⁴</td>
<td>Lucent (1998)</td>
</tr>
<tr>
<td>Parylene</td>
<td>0.02~0.08</td>
<td>10³ ~ 10⁴</td>
<td>E-Ink (2000)</td>
</tr>
<tr>
<td>PVP</td>
<td>3</td>
<td>~10⁵</td>
<td>Infineon (2002)</td>
</tr>
<tr>
<td>SiO₂ (OTS)</td>
<td>0.5~1.5</td>
<td>~ 10⁸</td>
<td>Penn. St (2001)</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>5</td>
<td>~10⁶</td>
<td>3M (2003)</td>
</tr>
</tbody>
</table>

* All based on Pentacene deposited under same condition
** S1; Samsung Advanced Institute of Technology

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### Development of New Organic Gate Insulator: S1

1. Typical 2D nucleation growth behavior
2. Grain size is about 2~3 μm
3. Thin film phase is dominant

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![Image of SEM images and spectrum](image-url)
Effect of deposition condition

- Dep. rate ~ 0.2 Å/sec
- Dep. rate ~ 1.5 Å/sec
- Dep. rate is a dominant control factor for on/off ratio.
- Mobility is more sensitive to dep. temperature at lower dep. rate.

Development of New Gate Insulator: S2

- Modification of Gate Dielectric for Pentacene OTFT
  - Gate dielectric: chemical resistance (etchant, PR stripper, etc)
  - Gate dielectric (S1) \( \Rightarrow \) cross-linking polymer blend (S2)
  - Dielectric coating \( \Rightarrow \) chemical treatment \( \Rightarrow \) TFT Fab. (Top contact)

<table>
<thead>
<tr>
<th>sample</th>
<th>SAIT1 (wt%)</th>
<th>Acrylate (wt%)</th>
<th>Mobility (cm²/Vs)</th>
<th>On/Off Ratio</th>
<th>Etching Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>100</td>
<td>0</td>
<td>5.4</td>
<td>( \sim 10^5 )</td>
<td>bad</td>
</tr>
<tr>
<td>#2</td>
<td>80</td>
<td>20</td>
<td>4</td>
<td>( \sim 10^6 )</td>
<td>good</td>
</tr>
<tr>
<td>#3</td>
<td>50</td>
<td>50</td>
<td>3.2</td>
<td>( 10^5 \sim 10^6 )</td>
<td>good</td>
</tr>
<tr>
<td>#4</td>
<td>20</td>
<td>80</td>
<td>0.2</td>
<td>( \sim 10^8 )</td>
<td>good</td>
</tr>
<tr>
<td>#5</td>
<td>0</td>
<td>100</td>
<td>0.01</td>
<td>( \sim 10^8 )</td>
<td>good</td>
</tr>
</tbody>
</table>
TR characteristics of Top Contact-type TFT

\[ I_d = \frac{W}{2L} \mu C_i [2(V_g - V_{th})V_d - V_d^2] \]

\[ \sqrt{I_{sat}} = \sqrt{\frac{Z}{2L}} \mu C_i (V_g - V_t) \]

TR characteristics of Bottom Contact-type TFT

4" OTFT Array Characteristics
Current Status & Future Work

Goal: For the Successful Business of “Large Sized Plastic AM Displays”

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<th>Materials</th>
<th>Current</th>
<th>Future</th>
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<tbody>
<tr>
<td>Semiconductor</td>
<td>Si TFT</td>
<td>Solution based OSC</td>
</tr>
<tr>
<td>Insulator</td>
<td>Inorganic (SiNx, SiOx)</td>
<td>Wet-processible</td>
</tr>
<tr>
<td>Bus Line</td>
<td>Metal (Cr, Al, Mo…)</td>
<td>Synthetic Metals, CNT</td>
</tr>
<tr>
<td>Electrode</td>
<td>ITO, IZO…</td>
<td>Conducting Organics</td>
</tr>
<tr>
<td>Process</td>
<td>Layer Process</td>
<td>Deposition, Evaporation, Spin Coating</td>
</tr>
<tr>
<td></td>
<td>Spinless or Roll Coating, Printing</td>
<td></td>
</tr>
<tr>
<td>Patterning</td>
<td>Photolithography, Shadow Mask</td>
<td>Inkjet or Micro-contact Printing, Soft-lithography</td>
</tr>
</tbody>
</table>

Future of Flexible Display

Development of Display for “Paper-Like Price” without Lowering of Image Quality...

► Extremely Low Cost as “$1/inch by 2010”

.. Not Simply Making Roll-up Display But Leading "Paradigm Shift of the Display Industry"