Single Soft-Switching Multi-Level Energy Recovery Circuit Driver for Plasma Display Panel

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ABSTRACT

The power source of an AC-PDP for sustainer circuit is operated in high-voltage and high frequency switching during the process required to achieve the gas discharge current to generate light in a PDP panel. Since PDP has the characteristics of a pure capacitive load, the displacement current that occurs during charge and discharge generates considerable reactive power. An auxiliary circuitry called Energy Recovery Circuit (ERC) reduces the capacitive displacement current. However, this auxiliary topology also bears high stress in its components. In this paper, a multilevel voltage wave shaping sustainer circuit with auxiliary ERC characteristics for an AC-PDP driver is proposed. A comparative analysis and experimental results are presented.

1. INTRODUCTION

The plasma display panel (PDP), has many desirable advantages over other competing flat panel displays and is expected to be the most promising flat panel display of the next generation [1, 2]. Due to the construction of the PDP, a dielectric layer exist between surface discharging electrodes and also between opposed discharging electrodes, therefore an intrinsic capacitance $C_p$ exist [3-5]. Thus, when applying a sustain pulse on the electrodes for charging and discharging the inter-electrode capacitor, the energy supplied from a power source is: $P = C_pV_d^2$, where $C_p$ is the equivalent panel capacitance and $V_d$ is the source voltage.

The common architecture used as sustainer driver circuit is based on a full-bridge inverter configuration and is implemented by Y and X driver board type [1]. As the PDP has the characteristics of a pure capacitive load, the displacement current that occurs during charging and discharging the PDP panel causes a considerable energy loss [1-5]. Furthermore, this surge current will give rise to EMI noises and increase the surge current ratings of power switches. If an inductor is placed in series with the panel, then $C_p$ can be charged and discharged through the inductor. This type of circuits is often called energy-recovery circuit (ERC). The main characteristic of the topologies classified as multilevel, is the use of commutation devices connected in series, allowing the distribution of the voltage and reducing stress in the commutation switches, so the use of less expensive components is feasible [6-8]. The proposed circuit features less device elements, voltage stresses and significantly reduced rms current stresses, compared with those of the conventional and multilevel ones.

2. OPERATIONAL PRINCIPLES

The common driving scheme for a plasma display panel (PDP) is the address-display-separation (ADS) method [9, 10]. The address period consists of a reset and address setup. The rest is the display period where the sustaining action is achieved. The proposed single driver and ERC in this article are based on Weber and Wood architecture [3-5]. Topology and key waveforms are shown in figure 1(a-b), respectively. For the analysis of the sustaining circuit operation, the following assumptions are made:

- The voltage of the input capacitors is considered as constant voltage $V_d/4$.
- The input capacitor values are equal; $C_1 = C_2 = C_3 = C_4 = C$.
- The input capacitance is much larger than the panel capacitance; $C_p << C$.
- The switches $S_1$, $S_3$, $S_{ML}$ and $S_{MD}$ are considered ideal except for $R_{ds-on}$.

Figure 2 shows the operational modes and the current path for each case of the proposed circuit.

Mode 1 ($t_0 < t < t_1$) Precharge Mode: Switch $S_{SW}$ is closed and therefore the energy stored in $C_4$ and $L_{ERC}$ is transferred to $C_P$ via path $C_P - S_{SW} - D_{SW} - L_{ERC} - C_P$ in a resonant mode. Then, the current through $L_{ERC}$ and voltage panel $C_P$ are:

$$I_{SW}(t) = \frac{V_d}{4} \frac{1}{Z_1 \sqrt{1 - \frac{1}{Z_1^2}}} e^{-\frac{2\pi}{\omega} (t - t_0)} \sin \left( \frac{\pi}{Z_1} (t - t_0) \right),$$

$$V_C(t) = \frac{V_d}{4} \left( 1 - e^{-\frac{2\pi}{\omega} (t - t_0)} \right) \frac{1}{\sqrt{1 - \frac{1}{Z_1^2}}} \sin \left( \frac{\pi}{Z_1} (t - t_0) \right).$$

![Fig. 1 Schematic diagram and key waveforms of proposed circuit.](image-url)
where, 
\[ a_o = \omega \sqrt{1 - \xi^2}, \quad \xi = \frac{R_d}{Z}, \quad R_e = R_{o_2} + R_o \] 

Note that \( R_{o_2} \) is the channel resistance of switch and \( R_o \) is diode's forward voltage.

Mode 2 (t_1 < t < t_2) Gas-discharge Mode: Switch \( S_{dg} \) transfers the energy in \( C_1 + C_2 \) to \( C_P \) via path \( C_1 + C_2 - D_{dg} - C_P \). If the peak voltage reached in \( C_P \) in previous stage is:
\[ V_{c_{prev}} = \frac{V_x}{4} \left( 1 + \frac{e^{-\xi}}{\sqrt{1 - \xi^2}} \right). \]

Then, the difference between the peak voltage during \( t_1 < t < t_2 \) and the voltage in \( t > t_2 \) is as follows:
\[ \Delta V = \frac{V_x}{2} - V_{c_{prev}} = \frac{V_x}{4} - \frac{V_x e^{-\xi}}{\sqrt{1 - \xi^2}}. \]

Mode 3 (t_2 < t < t_3) PredischARGE Mode: Switch \( S_{da} \) is closed and therefore the energy stored in \( C_1 + C_2 \) is transferred to \( C_P \) via path \( L_{DG} - S_{da} - D_{a} - C_P \) in a resonant mode. Then, the current trough \( L_{DG} \) and voltage panel \( C_P \) are:
\[ I_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_2)} \right) \sin \left[ \omega (t-t_2) \right]. \]
\[ V_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_2)} \right) \cos \left( \omega (t-t_2) + \frac{\xi}{\sqrt{1 - \xi^2}} \sin \left[ \omega (t-t_2) \right] \right). \]

Mode 4 (t_3 < t < t_4) Multi-chARGE Mode: Switch \( S_{DA} \) is closed and therefore the energy stored in \( C_1 + C_2 \) is transferred to \( C_P \) via path \( L_{DG} - S_{DA} - D_{a} - C_P \) in a resonant mode. Then, the current trough \( L_{DG} \) and voltage panel \( C_P \) are:
\[ I_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_3)} \right) \sin \left[ \omega (t-t_3) \right]. \]
\[ V_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_3)} \right) \cos \left( \omega (t-t_3) + \frac{\xi}{\sqrt{1 - \xi^2}} \sin \left[ \omega (t-t_3) \right] \right). \]

Mode 5 (t_4 < t < t_5) Gas-discharge Mode: Switch \( S_{DG} \) transfers the energy in \( C_1 + C_2 \) to \( C_P \) via path \( S_{DG} - D_{DG} - L_{DG} - C_P \) in a resonant mode. Then, the current trough \( L_{DG} \) and voltage panel \( C_P \) are:
\[ I_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_4)} \right) \sin \left[ \omega (t-t_4) \right]. \]
\[ V_{c_{DG}}(t) = \frac{V_x}{4} \left( 1 + e^{-\omega (t-t_4)} \right) \cos \left( \omega (t-t_4) + \frac{\xi}{\sqrt{1 - \xi^2}} \sin \left[ \omega (t-t_4) \right] \right). \]

It is noted that in Mode 2 and Mode 5 the immediate change of the panel voltage is a significant source of oscillations in the panel waveforms and therefore, causing switching power losses. This change, in the case of Mode 2, is defined as follows:
\[ \Delta V = \frac{V_x}{4} \left( 1 + e^{-\xi} \right). \]

3. COMPARATIVE ANALYSIS

The proposed architecture features less device voltage stresses compared with those of the conventional circuit [5] and similar to another multilevel sustaining driver [8].

3.1. Conduction Losses and Stress on Devices

For fair comparison, all the device voltages and currents ratings were based on the architecture diagram (showing in fig. 1), and using the conditions imposed in [4, 5, 8]. Table 1 shows the comparison of the component number and device stresses. The gas-discharge peak-current in the PDP is defined as \( I_{c_{DG}} \). It is easy to note that, as in [8], the peak voltages as well as the rms values of each device current are appreciably reduced in the order of a half. However, it is imperative to note that the part count numbers used are six for the proposed circuit, eight for another multilevel topology and four for the conventional circuit. Thus, it is expected that the proposed architecture achieve a superior performance not just by the part count number, moreover due to the absence of a side-2 sustaining driver. As can be distinguish (Table II), the power losses are larger reduced due to the count part number.

3.2. Switching Losses

The immediate change of the panel voltage, (eq. 9), is a significant source of oscillations in the panel waveforms and therefore, causing switching power losses.

By performing similar analysis, we can obtain the turn-off losses in the sustaining switches as:
\[ P_{off} = 2 (C_{p} + C_{e}) \cdot V_{c_{DG}}^2 \cdot f \cdot \# devices \]
\[ = \frac{(C_{p} + C_{e})}{2} \cdot V_{c_{DG}}^2 \cdot f \cdot \left( 1 - \frac{e^{-\xi}}{\sqrt{1 - \xi}} \right) \cdot \# devices. \]

In addition, the turn-on switching losses on the ERC switches are as follows:
\[ P_{on} = \frac{C_{e} + C_{p}}{2} \cdot V_{c_{DG}}^2 \cdot f \cdot \# devices \]
\[ = \frac{C_{e} + C_{p}}{4} \cdot V_{c_{DG}}^2 \cdot f \cdot \# devices \]

where \( C_{e} \) and \( C_{p} \) are the inherent capacitances of the sustain switch and panel, respectively, and \( C_{e} + C_{p} \) is the drain to source capacitance of the ERC switches. Is expected that switching loss of the proposed circuit is smaller that the previous proposed circuits.

4. EXPERIMENTAL RESULTS

Figure 3(a-d) shows the correspondent experimental results using a pure capacitance; gate signals are FPGA-based. As seen in figure 3(c-d), it is noted that the turn-on switching losses can be negligible since the switches \( S_{DG}, S_{DA}, S_{MD} \) and \( S_{MD} \) operate nearly under the zero voltage switching condition.
4.1. Practical Implementation

In order to validate the features of the proposed topology, a prototype is implemented to drive a 42" PDP. As considered in [8, 9], the duration of $T_{\text{dis}}$ can be arbitrarily chosen in the range of 1.7–2.5μsec, to be longer than the gas discharge extinction time. Figure 4 shows the experimental waveforms for a 42" PDP. It is easily appreciated in this breadboard prototype the gas discharge current and the capacitive displacement waveform.

5. CONCLUSION

The comparative analysis gives a fine reason to consider this circuit as an alternative architecture related on multi-level sustaining drivers for plasma panels without much increased number of semiconductor devices. Therefore, it is reasonable to consider this circuit as a good candidate for a design of a low-cost high-power-density AC-PDP driver.

**TABLE I**

DEVICE NUMBER & STRESS COMPARISON

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<td>6</td>
<td>16</td>
<td>8</td>
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**Sustain switch**
- peak voltage $V_{\text{p,k,dc}}$ 0.5$V_s'$ 0.5$V_s'$ $V_s$
- peak current $I_{\text{p,k,dc}}$ $I_{\text{gss}}$ $I_{\text{gss}}$ $I_{\text{gss}}$
- RMS current $I_{\text{rms,k,dc}}$ $V_s' / 4 \sqrt{1 / 2}$ $V_s' / 4 \sqrt{1 / 2}$ $V_s' / 4 \sqrt{1 / 2}$ $V_s' / 4 \sqrt{1 / 2}$ $\ldots$

**ERC switch**
- peak voltage $V_{\text{p,k,dc}}$ 0.25$V_s'$ 0.25$V_s'$ 0.5$V_s'$
- peak current $I_{\text{p,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$
- RMS current $I_{\text{rms,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $\ldots$

**ERC Diode**
- peak voltage $V_{\text{p,k,dc}}$ 0.25$V_s'$ 0.25$V_s'$ 0.5$V_s'$
- peak current $I_{\text{p,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$
- RMS current $I_{\text{rms,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$
- average current $I_{\text{ave,k,dc}}$ 0.5$V_s'$ 0.5$V_s'$ $V_s' / 2Z_s'$

**Inductor**
- RMS current $I_{\text{rms,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $\ldots$

**Capacitor**
- peak voltage $V_{\text{p,k,dc}}$ 0.25$V_s'$ 0.25$V_s'$ 0.5$V_s'$
- RMS current $I_{\text{rms,k,dc}}$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $V_s' / 4Z_s'$ $\ldots$

**Clamp diode**
- peak voltage $V_{\text{p,k,dc}}$ $\ldots$ 0.5$V_s'$ $\ldots$

**TABLE II**

CONDUCTION LOSS COMPARISON

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<td>Reactive Power $P_r$</td>
<td>0.5$C_s' V_s'^2 f$</td>
<td>0.5$C_s' V_s'^2 f$</td>
<td>$C_s' V_s'^2 f$</td>
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<td>ERC switches $I_{\text{rms,k,dc}} R_{\text{rms,k,dc}}$ $\varphi$ dev.</td>
<td>$V_s'^2 / 32 Z_s'^2 \cdot T_s \cdot f \cdot R_{\text{rms,k,dc}}$</td>
<td>$V_s'^2 / 16 Z_s'^2 \cdot T_s \cdot f \cdot R_{\text{rms,k,dc}}$</td>
<td>$V_s'^2 / 32 Z_s'^2 \cdot T_s \cdot f \cdot R_{\text{rms,k,dc}}$</td>
</tr>
<tr>
<td>ERC Diode $I_{\text{rms,k,dc}} R_{\text{rms,k,dc}}$ $\varphi$ dev.</td>
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<td>$V_s'^2 / 16 Z_s'^2 \cdot T_s \cdot f \cdot R_{\text{rms,k,dc}}$</td>
<td>$V_s'^2 / 32 Z_s'^2 \cdot T_s \cdot f \cdot R_{\text{rms,k,dc}}$</td>
</tr>
<tr>
<td>Sustain switches $I_{\text{rms,k,dc}}$ $R_{\text{rms,k,dc}}$ $\varphi$ dev.</td>
<td>$0.7 C_s' V_s'^2 f$</td>
<td>$0.7 C_s' V_s'^2 f$</td>
<td>$0.7 C_s' V_s'^2 f$</td>
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**Fig. 4** Prototype of 42" PDP with MOSFET's.

**REFERENCES**


