Development of high speed image acquiring system of a confocal microscope for High Contents Screening

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1. Introduction

The main application of a confocal microscope (CM) in the biology and the biomedical sciences is to image either fixed or living tissues which have labeled with one or more fluorescent probes.

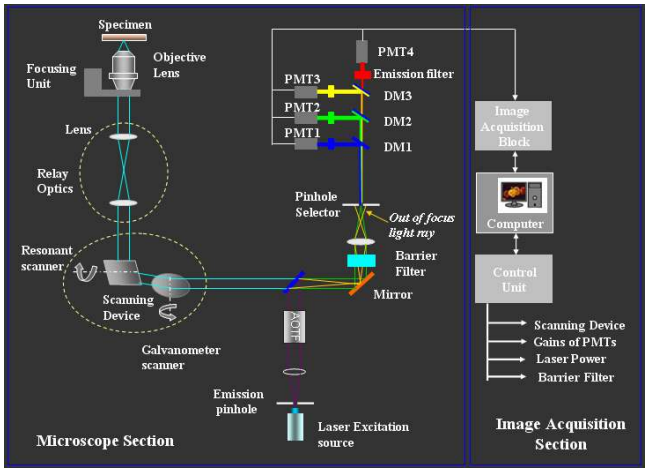

Figure 1: The block diagram of a confocal system

The confocal principle Coherent light emitted by the laser system (excitation source) passes through a pinhole (Emission Pinhole) aperture that is situated in a conjugate plane (con-focal) with a scanning point on the specimen and a second pinhole (Pinhole Selector) aperture positioned in front of the detectors (PMTs). As the laser is reflected by a dichromatic mirror and scanned across the specimen in a defined focal plane, secondary fluorescence emitted from points on the specimen (in the same focal plane) pass back through the dichromatic mirror and are focused as a confocal point at the detector pinhole aperture through a Pinhole Selector. It prevents light from above or below the plane of focus not to strike upon PMT (termed Out-of-Focus light Rays in Fig.1).

The high content screening (HCS) is a drug discovery method that uses images of living cells as the basic unit for molecule discovery, it describes the use of spatially or temporally resolved methods to multiple informational vectors in parallel, thereby allowing integrated analysis approaches.

To develop CM for HCS, we have proposed the method to design the high speed image acquiring system for increase the rate of images per second by simultaneous imaging of four fluorescent color channels (Blue, Green, Red, and Yellow) with high resolution of image data up to 12 bits, and automatic accurate control its peripherals, which contribute to form images of a specimen, such as a scanning device, PMT, and laser source by program on a computer for having the image speed is 30x4 frames per second.

2. Materials and Methods

2.1 Processing the synchronous output signals of the scanning device

To process the synchronous signals from scanning device, The FPGA chips of Altera Corporation in company with the programming environment Quatus II were selected. All triggered events of Pixel Clock, Pixel Enable, Phase Lock pulses such as falling edges and rising edges were captured based on Pixel Clock, which is the global clock (the FPGA block diagram on Fig.2). By using the counters and logical complex block, The Pixel Clock pulses are gated by Pixel Enable pulses with the constant number of pixel a line, the Pixel Enable pulses are gated by Phase Lock Pulse to form the number of lines per an image frame (the timing chart Fig.2). The function blocks like counters and logical complex block of FPGA chip can easily be programmed by using programming languages such as text (VHDL) or graphic or timing chart, so the firmware inside FPGA chip can compensate few deficient pulses, in the case that scanning device works incorrectly, to fix enough the number of pixel per line and the number of lines per image frame. The corrected synchronous signals on outputs of FPGA were changed to enable signals of standard camera-link such as: DVAL, LVAL, and FVAL. The Pixel Clock is frequently multiplied by 7 times, and then it samples the DVAL, LVAL, FVAL and data of a pixel (up to 12 bits) to packing standardly and send to frame grabber, which is being used standard camera-link protocol. These functions could easily be implemented by the single channel Link chip family such as DS90CR287 converting to the LVDS signals.

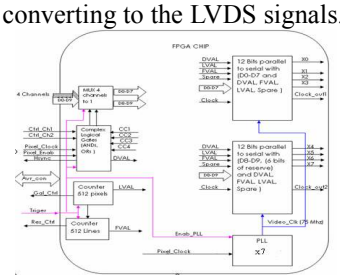

Figure 2: The block diagram and timing chart of the FPGA board

2.2 The method to speed the rate of images by parallel data processing of four PMT channels

These enable signals are combined with 10-bit digital data on 4 channels (10-bit words D0, D1, D2, and D3) appropriately with the values of output analogue signals of 4 PMT. To grab concurrently image data of 4 channels (speed up the rate of frame per second), the 10-bit data of 4 channels (10-bit words D0, D1, D2, and D3), which were sampled and processed during each Pixel Clock signal by ADC and FPGA chip, have to be passed all to the 8 bytes in the image data buffer in a frame grabber connected to a computer via PCI standard. By analysis of the protocol of camera-link standard, the full configuration, which is used 8 ports (A, B, C, D, E, F, G, H), converted to LVDS signals by 3 Channel-link chip DS90CR287A in FPGA board and converted again to image data by DS90CR288 built in a frame grabber (Fig. 3), has to be implemented. The image processing program on a computer can easily grab the image

data in the buffer (8 bytes image data) and display images of the specimen on 4 color screens (Red, Blue, Green, and Yellow) correspondingly with 4PMTs. The image acquisition prototype could be easily used with any kind of frame grabbers, which use the protocol of camera-link standard. In this prototype the frame grabber Matrox Solios eV-CL was used in the single full configuration. The image processing program in environment visual C++ separately decoded the image data in the buffer library of MIL (Matrox Imaging Library) and collected to display on 4 screens. This method is implemented by the FPGA board (Fig.3).

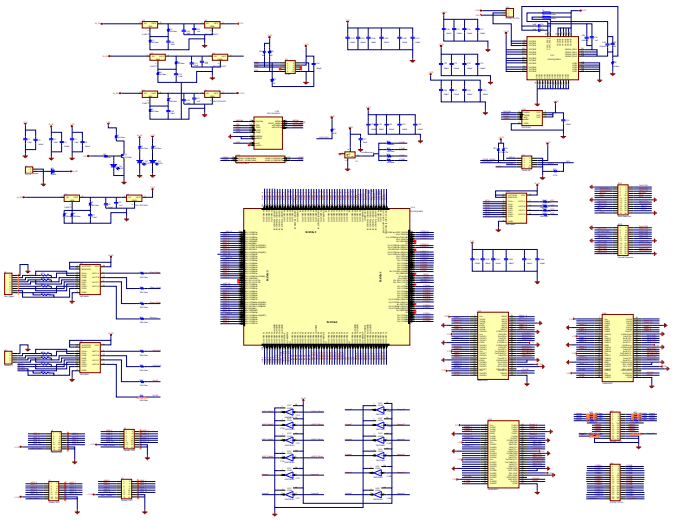

Figure 3: *The FPGA board process the synchronous signals forming to the enable signals of the camera-link standard.*

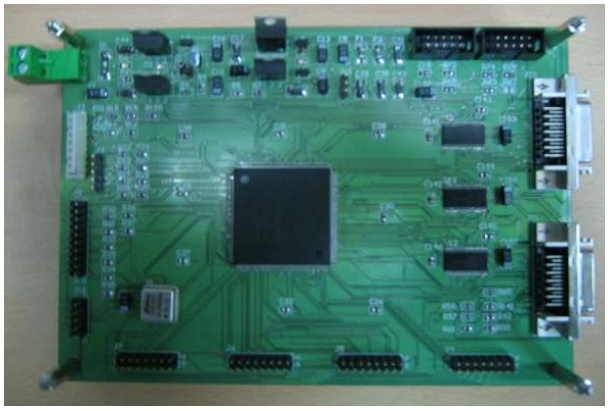

Figure 4: *The PCB FPGA board.*

2.3 Controlling signals for a scanning device, and PMTs and other peripherals

The synchronous signals are very important to frame an image on a computer. However, these signals are closely relative to the controlling signals on input of scanning device such as the galvanometer control signal (Gal_control), the resonance control signal (Res_control), and the enable signal announced in a datasheet of the scanning device. Especially, the value of the amplitude of Res_control directly affects to Pixel Enable, Phase Lock, and frequency of Pixel Clock, and the Gal_control controls the reflecting region of light beam focused in Pinhole and PMT. Therefore, the requirement of these signals is accurate. The microcontroller and parallel high-speed DAC were proposed for making controlling signals for the scanning device. The amplitude of controlling signals could be changed in the voltage range (0-3V) by commands from a computer using the protocol of UART.

The Gains of PMTs were unnoisily accurately adjusted in the small range from 0 to 0.9 V (the specification of manufacturer, who made the PMT) by using serial low noise high speed DAC 10-bit (inter-integrated circuit bus DAC10) with 1024 voltage levels and data-processing built in microcontroller Atmega128. Moreover, they were made extremely low noise (noise level is less than 10 mV) by using the integrated method of techniques for countermeasure noise.

3. Results

The acquired images could meet the goal of high peed acquiring system for high content screening. The photon signals of four PMTs channels were parallely processed to store in the memory of a computer supporting image data for discovery the cellular properties in HCS system. By using the specimen on well-plate with four laser excitation sources, the images on four screens were displayed like figure 5.

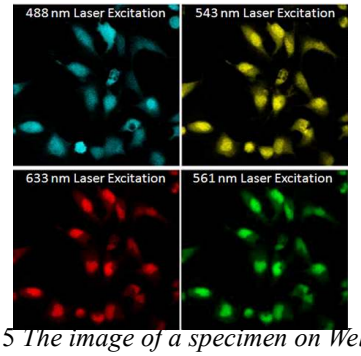

Fig. 5 *The image of a specimen on Well-plate*

4. Conclusion

The rate of the image frames were up to 30 x4 frames per second. The new image acquiring system worked stably with the unstained images displayed, capability to integrate in Confocal Microscope for high content screening.

5. Discussion

Actually, the resonant scanner is only active in one-direction, the supplied device driver do not support for bi-diectional scanning. Therefore to increase the rate of frames, the backward direction of resonant should be considered.

6. Acknowledgement

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7. References

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