Efficient, scalable and compact DC Fast Charging Concept

**Agenda**

1. Motivation
2. Trends and requirements for DC Fast Charging
3. Analysis of optimized topology
4. Design considerations
5. Modular 50kW power cell
6. Summary
1) Motivation

Increasing pollution, new advances in battery technology and a global demand of emission control pave the way for the **transition to electrical vehicles**.

But wide-spread EV adoption is constrained by concerns of consumers regarding **charging infrastructure**. Major concerns are:
- Scarcity of charging locations
- Too slow charging speed

Worldwide, governments and industries are preparing to invest in charging infrastructure but critical points are **cost, power and reliability**.

In this presentation we analyze a cost efficient topology of a **modular 50kW power cell** for fast charging up to 350kW. We address demands of industry and governments by
- **low cost**,  
- **high efficient** and  
- **reliable** system design

2) Trends and requirements – Power ratings

- **Home & Office:**
  - Slow charging
  - AC charging

- **Public & Retail**
  - Fast charging
  - DC charging

- **Highway**
  - High power charging
  - Fast DC charging

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2) Trends and requirements – Key Drivers for DC Fast Charger

**Power ratings:**
- 50kW – 350kW
- 400Vdc – 1000Vdc

**Form factor**
- Small footprint for inner city installation

**Volume benefits:**
- Modularity creates scale and flexibility

**Cost development:**
- Global price pressure
- 20 years functional

![Graph showing charging time for 400km @ 80% SoC](image)

3) Topology – 50kW Power Cell

**50kW Power Cell requirements**
- Compact design
- PFC
- Isolation for safety
- Periphery / interface
- Design for manufacturing

**Specification**
*all following tests and simulation are based on this spec*

- **Power Rating:** 50kW
- **AC Input:** 400 V ± 10 %
- **DC Output:** 500Vdc or 1000Vdc
- **Fsw:** 40kHz
- **PF:** >0.98
- **Efficiency:** >97%

![Typical EV Power Electronics Topologies](image)
3) Topology – AC-DC topology

**Diode rectifier**
- Simple
- Cost efficient
- Bad THD
- No voltage control

**Active Front End**
- PFC in boost mode
- Bi-directional possible
- Low efficiency (1200V)
- Low switching speed
  (option: SiC but at cost)

**Three Level PFC**
- High efficiency
- Cost efficient
- DC-Link center point
- 6 instead of 12 channels

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3) Topology – Comparison of chipsets

<table>
<thead>
<tr>
<th>Fast IGBT / SI Fast Diode</th>
<th>SI MOSFET / SiC Diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1/T2 Fast IGBT</td>
<td>T1/T2 Si MOSFET</td>
</tr>
<tr>
<td>D1/D4 Fast Si Diode</td>
<td>D1/D4 SiC Diode</td>
</tr>
<tr>
<td>D2/D3 Rectifier diodes</td>
<td>D2/D3 Rectifier diodes</td>
</tr>
<tr>
<td>D5/D6 Protection diodes</td>
<td>D5/D6 Body diode</td>
</tr>
</tbody>
</table>

![Graph showing comparison of leveled cost and efficiency between Fast IGBT / SI Fast Diode and SI MOSFET / SiC Diode.](image)

- **Levelized cost**
  - Fast IGBT / SI Fast Diode: 100%
  - SI MOSFET / SiC Diode: 152%
- **Efficiency**
  - Fast IGBT / SI Fast Diode: 98.22%
  - SI MOSFET / SiC Diode: 98.71%

One phase-leg of the three Level PFC

**P=50kW, Fsw = 40kHz**

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3) Topology – Isolated DC/DC Converter

**Series connected B2I**
- DC-Link center point allows series connection of B2I
- 650V IGBTs for low static and dynamic losses
- Flexible DC output: 500Vdc or 1000Vdc
- Optimized HF transformer at 40kHz

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2 x B2I + HF Transformer + 2 x B2U

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3) Topology – Comparison of chipsets

**Comparison for fast switching 650V IGBTs:**
- Chipsets
- Module platforms

**Focus:**
- Low static and dynamic losses
- Low inductive design
- Optimized chip layout

**Comparison of losses**

<table>
<thead>
<tr>
<th>650V IGBT IFX</th>
<th>HS</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CE(on)}$ @25°C</td>
<td>1,65 V</td>
<td>1,35 V</td>
</tr>
<tr>
<td>$V_{CE(on)}$ @150°C</td>
<td>2,1 V</td>
<td>1,7 V</td>
</tr>
<tr>
<td>$E_{on}/100A$ @150°C</td>
<td>2,3 mJ</td>
<td>2,5 mJ</td>
</tr>
<tr>
<td>$E_{on}/100A$ @150°C</td>
<td>1,5 mJ</td>
<td>1,1 mJ</td>
</tr>
<tr>
<td>$E_{on}/100A$ @150°C</td>
<td>0,8 mJ</td>
<td>1,4 mJ</td>
</tr>
</tbody>
</table>
4) Design considerations - Fast switching

**What is fast switching**

- 10-40 kHz
  - 600V / 1200V
  - New Si chips, new topologies, hybrid SiC
  - No significant impact on module/system

- >40 kHz
  - 1200V/1700V
  - SiC
  - New challenges on module/system

**Benefits:**
- Increase efficiency
- Improve modulation accuracy
- Reduction of costs
- Reduction of size

![Graph showing fast switching with 30kV/µs and 2ns stray inductance](image)

4) Design considerations - Stray inductance

**Stray inductance**

- Over voltage during switch-off over IGBTs/MOSFETs
- Oscillations with chip capacitance –EMI
- Overtoltage limits switching loss reduction by small $R_G$
- Maximum usable DC link is limited

![Diagram showing maximum blocking voltage of IGBT](image)

High $di/dt$ in short circuit condition!
4) Design considerations - Optimization for fast switching

**Considerations Module:**

- Use gate inductance as current booster during Miller plateau – the smaller is not necessarily better
- Optimize DC+ / - terminals regarding minimum stray inductance
- Optimize DBC design regarding chips, bonds, DBC layout

4) Design considerations - Low inductive DC link

**Considerations DC-Link:**

- Integrate snubber capacitors => DC Link-snubber oscillations
- Short distance between DC +/-
- Maximum overlap of DC+/-
- Paralleling of pins (power pins/ bars of module and capacitors)

\[ L_{\text{DCBusbar}} \approx \mu \times a \times d/b \]

\[ L_{\text{cap}} \approx L_{\text{single}}/\text{capacitors} \]
4) Design considerations - Efficient Driver Electronics

**Challenges Driver:**
- dV/dt > 100kV/µs with F_{SW} > 300 kHz
- Q_{G} ~ SI, F_{SW} + 300% -> I_{poutav} up to 1A
- T_{dead} lower as higher conduction losses when in reverse operation
- Fast V_{ce} detection required to avoid gate oxide damage
- Lower gate threshold voltage requires safe off-hold
- F_{SW} higher -> More impact of gate path inductance on oscillations

4) Design considerations – Industry standard package

**SEMITOP E2**
Industry standard package
Pin Grid structure allows flexible placing of the Press-Fit pins

**Optimized chip layout:**
- Lowest commutation inductance
  \[ L_{\text{stray}} = 6\text{nH} \]

**Super low inductive system design**
- \( L_{\text{stray,compl.}} = 10\text{nH} \)
  Vs. 45nH in std. module
  Perfect layout for paralleling
5) Modular 50kW power cell - Optimized topology

Three Level PFC

2 x B2I + HF trafo

2 x B2U

5) Modular 50kW power cell - Concept

Product scope

Topology

50kW Power Cell
5) Modular 50kW power cell - 350kW EV Charger

**SEMIKRON**

350kW Power
(7 x 50kW Power Cell)
Incl. galvanic isolation for safety

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**Example: 350kW EV HP-Charger**

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**Customer**

EV Charger controller,
Charging satellites and system integration

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**Summary**

**Optimized topology:**
- 3L PFC topology needs just 6 instead 12 driver channels
- Split DC link allows usage of cheap and efficient 650V technology
- Split of transformers allows best passive costs and scalability
- 40kHz switching frequency for optimal cost/performance
- Integrated pre charge circuit
- Lowest inverter costs reaching all targets like 97% efficiency

**Design efficiency:**
- Use of 650V IGBT technology
- Standard technology allows volume production
Thank you for your attention