자기 동조법에 의한 정현파 간섭음 제거

Sinusoidal Interference Rejection by Self-Tuning Method

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요 약

회로의 간편성에 최대 역점을 두어 PLL(phase locked loop)을 이용한 정현파 간섭음을 실시간으로 제거하는 방식을 제안하였다. SC(switched capacitor) 여파기를 이용한 적응 노치(notch) 여파기와 적응 대역 여파기를 자기 동조방법으로 구동시킴으로써 간섭음을 제거하였다.

SC여파기의 구동 스위칭 주파수는 제거하려는 신호 주파수의 49배가 되도록 하였으며 소자의 동작 특성상 4 KHz의 간섭음 제거 대역을 갖게 된다. 노치 여파기는 6차 여파기이고 감쇄도는 중심 주파수에서 약 −56dB이다.

ABSTRACT

It is proposed that the sinusoidal interference can be removed by using the PLL scheme in real-time. Adaptive notch and band pass filter are implemented using SC(switched capacitor) filter – so called self-tuning method. The switching freq. of SC filter is 49 times as large as the frequ. of interference signal, and the rejection frequency is in the ranges of 4 KHz.

The notch filter used here is the sixth order and shows the attenuation of -56dB at the notch point.

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I. INTRODUCTION

We have experienced a sinusoidal interference in many cases.

For example, hums and other noises of motor or engine are typical. The interference involving harmonics is more general than the purely sinusoidal, but in most cases a large portion of power is concentrated on its fundamental frequency.

There were many researches in this sinusoidal interference rejection problems [1-4]. If the sinusoidal interference is frequency-invariant, the problem is very simple. But unfortunately the interference signal has the frequency-varying property.

Therefore, the adaptive filtering method [1] [2] [4] has been chosen for this purpose, but this approach requires considerably complicate hardwares and, in general, processing of the signal in digital form.

In this paper, the scheme is proposed that is to have the notch center frequency adaptively tracted under the control of sampled frequency.

Sampled-data filters, or switched-capacitor filters have the common frequency characteristics which depends upon the switching clock rate.

In virtue of this fact, we can implement the tunable filter controlled by clock frequency. Thus the main problem is how to extract the interference signal from the input signal, which is added by unwanted interference signal.

The unwanted interference can be extracted by use of tunable BPF and PLL. After clock frequency is synthesized from this frequency of extracted interference signal, we can use this clock signal as the input to the tunable notch filter. Hereafter, we can have the useful sampling, or switching clock which tracts the frequency of interference signal.

II. SYSTEM DESCRIPTION AND SIGNAL ANALYSIS

In Fig. 1, the block diagram of the proposed system is shown.

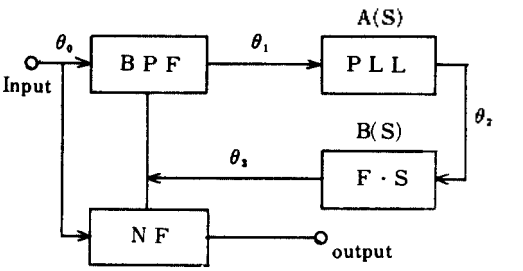

Fig. 1. Schematic system description

It is noted that BPF(band pass filter) and NF(notch filter) have the same characteristics of clock-controlled center frequency. The PLL A(s) will be chased to the BPF output in order to supply the F.S. (frequency synthesizer) with the squared input which is synthesized for the control clock of tunable BPF/NF.

The phase relationship between input phase θ_0 and driving phase θ_1 is investigated from the Figs. 1 and 2 as follows.

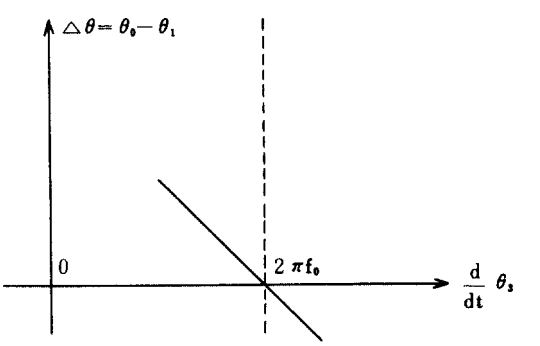

Fig. 2. Phase characteristics

$$f_o = \frac{1}{2\pi} \frac{d\theta_o}{dt} \tag{1}$$

If eq. (1) and the proportional constant k is used.

$$\theta_i - \theta_o = k\left(\frac{d\theta_i}{dt} - 2\pi f_o\right) = k\left(\frac{d\theta_i}{dt} - \frac{d\theta_o}{dt}\right) \tag{2}$$

The relationship between phase θ_i and phase θ_o in s-domain is determined as shown eq. (3)

$$\theta_o(s) = A(s)\,B(s)\;\theta_i(s) \tag{3}$$

, where A(s) is the transfer function of PLL,

B(s) is the transfer function of F.S.

Through the eqs. (4), (5) the desired phase relationship is appeared in eq. (6).

$$\frac{\theta_o(s)}{A(s)\,B(s)} - \theta_o(s) = ks\,\theta_o(s) - ks\,\theta_o(s) \tag{4}$$

$$\left(\frac{1}{A(s)\,B(s)} - ks\right)\theta_o(s) = (1 - ks)\;\theta_o(s) \tag{5}$$

$$\theta_o(s) = \frac{(1-ks)\;A(s)\;B(s)}{1 - ks\;A(s)\;B(s)}\;\theta_o(s) \tag{6}$$

Next, we have studied the lock and capture reaction to loop filter in PLL.

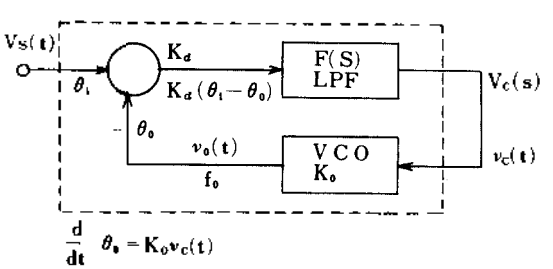

Fig. 3. PLL operating characteristics

In the following Fig. 3, the heuristic concept for the PLL operating characteristics can be perceived.

In Fig. 3, Kd is the phase detector conversion gain,

Ko is the VCO conversion gain.

In the first place, if the PLL input signal Vs(t) is equal to zero, VCO(voltage controlled oscillator) is in the state of free-running.

In turn, unless the input voltage Vs(t) is zero, the following procedure can be derived.

In the phase-locked state, the relationship between phase $\theta_o(s)$ and phase $\theta_i(s)$ can be expressed as shown in eq. (7).

$$\frac{\theta_o(s)}{\theta_i(s)} = H(s) = \frac{KoKd\;F(s)}{s + KoKd\;F(s)} \tag{7}$$

where H(s) is the transfer function of closed loop,

F(s) is the transfer function of loop filter-(LPF).

Thus,

$$1 - H(s) = \frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{\theta_e(s)}{\theta_i(s)} = \frac{s}{s + KoKd\;F(s)} \tag{8}$$

From the eqs.(7),(8) we can determine how the input phase is related to the VCO driving signal in s-domain.

$$V_c(s) = \frac{s\;Kd\;F(s)}{s + KoKd\;F(s)} \cdot \theta_i(s) \tag{9}$$

In general, the capture range is more narrow than the lock range. The mathematical relationship obviously shows the loop filter dependency.

The used loop filter circuit in this paper is

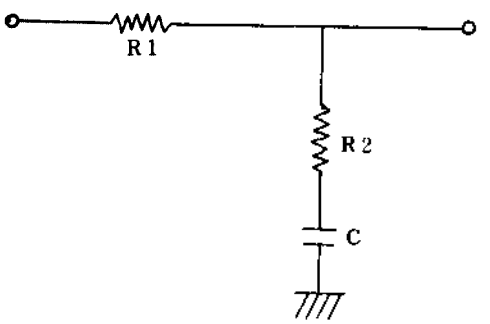

Fig. 4. Used loop filter circuit

shown in Fig. 4.

Also, it can be shown that the capture range, Wc, can be determined from eq. (10).

$$W_c \simeq W_L * \frac{R2}{R1+R2} \qquad (10)$$

where, W_L is lock range.

III. EXPERIMENTATION AND RESULTS

From Fig. 1, the output of BPF is the interference signal g(t), which is to be locked in PLL circuitry. At the locked-state the rectangular waveform for g(t) is produced at the output of VCO.

In turn, this signal is input to F.S(frequency synthesizer) whose output has the frequency, fs.

$$f_s = f_c * 49.23 \qquad (11)$$

where, fs is switching freq. driving tunable NF/BPF,

fc is center freq. of tunable NF/BPF.

The frequency responses of the notch and band pass filter are shown in Fig. 5, Fig. 6.

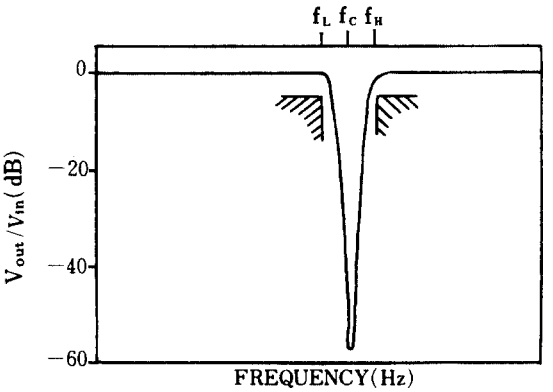

Fig. 5. Notch filter characteristics

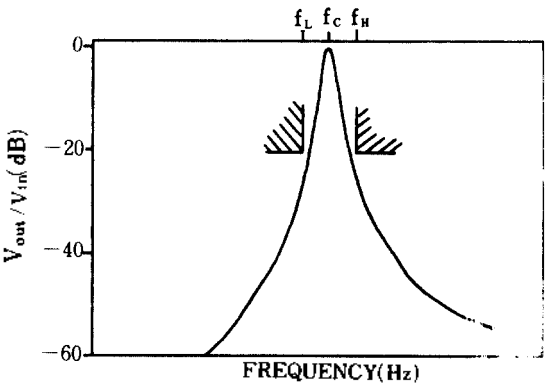

Fig. 6. BPF characteristics

In Fig. 5, $f_C = f_S/49.23$

$f_L = f_S/58.2$

$f_H = f_S/45.71$

In Fig. 6, $f_C = f_S/49.23$

$f_L = f_S/57.9$

$f_H = f_S/48.2$

And the quality factor Q is about 26, 3dB BW $= fs/1295$.

The frequency synthesizer can be implemented as shown in Fig. 7.

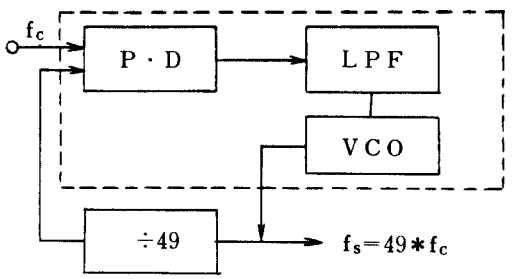

Fig. 7. Frequency synthesizer

Though the wanted switching frequency fs is fc*49.23, the experimentally used switching freq. fs, is fc*49 since we have implemented the frequency synthesizer by use of PLL and TTL counter to use less devices as possible. Though, we can obtain the satisfiable result.

And the used parameters can be sought through the following procedure.

$$f_o = 0.3 / (R * C1) \ [Hz] \quad (12)$$

$$f_L = \pm 8 * f_o / V_{cc} \ [Hz] \quad (13)$$

$$f_c \cong \pm SQRT\{2 * \pi * f_L / r\} / (2 * \pi) \ [Hz] \quad (14)$$

wherer is equal to 3600*C2,

R is used for VCO, $(2k < R < 20k)$

C1 is the connected capacitance to VCO.

C2 is the capacitance connected between Vcc and VCO control voltage pin in PLL NE565,

fo is free-running freq. of VCO,

$2 * f_L$ is the locking range,

$2 * f_c$ is the capture range.

In Fig. 8, the upper signal is the output of notch filter in case of any message and the lower is the output of BPF which is randomly proposed interference (625kHz).

Fig. 9 shows the spectrum of BPF output for the lower signal in Fig. 8.

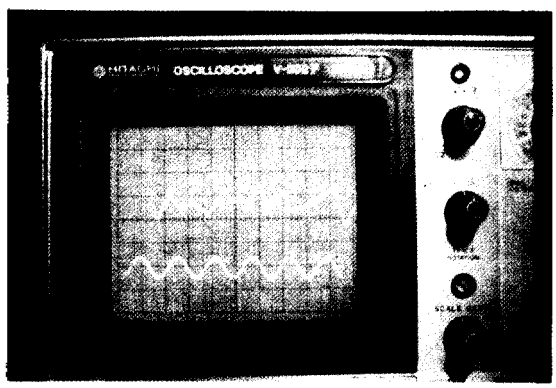

Fig. 8. Outputs of NF & BPF

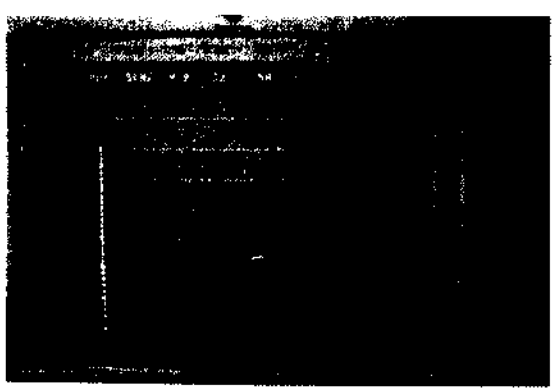

Fig. 9. Spectrum of BPF output

IV. CONCLUSION

Magnitude- and frequency-varying sinusoidal interference which we have frequently experienced in DSB-AM or SSB receiver can be rejected by use of this proposed simple circuit system in analog base up to 4 KHz since the used SC filter has the limit of operating frequency characteristics.

The proposed circuit is based upon the self-tuning method, i.e. tunable notch and band pass filter whose center frequency are the same.

The about -56dB attenuation can be obtained at notch point with 6 order as shown in Fig. 5.

The results of this paper will be used for the enhancement of communication receiver performances.

Next research will be directed to the expansion of rejection frequency range. (up to total audible frequency limit, 20kHz)

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