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〈연구논문〉

Strain Relief of Ge_xSi_{1-x} on Si(100) Mesa Structure

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Si(100) 메사 구조위에 성장시킨 Ge_xSi_{1-x} 층에서의 응력 풀림

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Abstract — We made mesa structures with the width ranging from submicron to 50 μm in order to investigate the mechanism of enhanced strain relieving of strained layer grown on small substrates. We also performed micro Raman spectroscopy, XPS, I-V and C-V measurement in order to study the strain relieving in Ge/Si growth on mesa structure. Elastic strain is relieved substantially when a Ge_xSi_{1-x} layer was grown on mesa structure, comparing the Ge_xSi_{1-x} layer grown on a plain Si. The strain relief at mesa structure was related to the nucleation of elastic dislocation at the edge of mesa structure.

요 약 — 기판의 크기에 따른 Strained Layer에서의 응력 풀림 현상을 연구하기 위하여 마이크론 이하에서 50 마이크론의 크기를 가지는 메사 구조를 제작하였다. 제작된 메사 구조위에 성장시킨 GeSi층은 마이크로 Raman, XPS, I-V와 C-V측정에 의하여 응력의 풀림현상을 관찰하였다. 이 실험을 통하여, 메사구조 위에 성장시킨 Ge_xSi_{1-x} 층에서의 응력 풀림이 편평한 기판위에 성장시킨 경우에 비하여 원활하였다. 이것은 메사 구조의 가장자리의 Strain Dislocation이 편중되는 것으로 이해될 수 있다.

1. Introduction

The fabrication of a dislocation free hetero-epitaxial layer is the main goal for epitaxial successful devices. The earlier elastic theory by Frank and van der Merwe proposed strained heteroepitaxial layer with the lattice mismatch of less than 15% and the thickness of less than critical thickness, t_c [1]. When the lattice mismatch exceeds the 15% or the thickness does over t_c, misfit dislocation is developed in the epitaxial layer. The onset of creation of misfit dislocation is caused by the increase of strain energy with thickness and the total energy is increased by strain energy with thick ness while it is lowered by misfit dislocation. Dislocations are usually nucleated at interface, surface and defects. Recently, much effort has been made to obtain epitaxial layer with low dislocation density.

Several methods of growth can be used to grow the dislocation free heteroepitaxy layer. One way to grow dislocation free layers is the alternating growth of substrate and overlayer layers [2]. The thickness of each layer is controlled to be thinner than the critical thickness. The layer is usually grown without dislocation up to several thousand angstrom. Another way to control the nucleation of dislocation at the interface is the use of surfactant [3]. The surfactant layer lowers the interface energy, therefore it inhibits the growth of

dislocation. The growth of thick dislocation free epitaxial layer has been reported with the use of surfactants. These two methods limit the strain energy at the interface by using multilayer growth and surfactant. Recently, a new method to localize the dislocation near specific site has been developed [4]. By intentional design of site where the dislocation can be bunched, the other areas are free of dislocation. Therefore, the strain can be relieved by growing on small substrate. As very-large-scale-integrated-circuit (VISI) with submicron size is widely used, the growth mechanism of this can be utilized. The growth behavior on a small substrate has drawn much attention to understand.

We have performed the experiment to understand the strained grown layer on patterned mesas. Ge/Si(100) system was chosen to study growth behavior of the strained layer. The system has been chosen as a candidate of high speed device, if dislocation free layers can be grown.

The samples used in this experiment were cut from 2~5 Ω·cm As-doped Si(100) wafer. In order to obtain the microscopic picture for the critical thickness, we performed the experiment using ultrahigh vacuum scanning tunneling microscope (UHV STM). The details of STM used in this experiment can be found elsewhere [5]. The molecular beam epitaxy (MBE) chamber equipped with UHV STM for the characterization of the grown layer with atomic resolution was used in this experiment. The base presure of the chamber was $<2\times10^{-10}$ Torr, and $<1\times10^{-9}$ Torr with the deposition source on. Micro Raman, XPS, current-voltage (I-V) and capacitance-voltage (C-V) dependence study were done after the sample was removed from the chamber. The mesa structure was made by photolithography with widths of mesa structures ranging from 0.3 μm to 50 μm. The patterned samples coated by photo-resist(PR) were etched by the dry etching process, follwed by PR stripping. The heights of mesa structures were prepared to be higher than 1 μm.

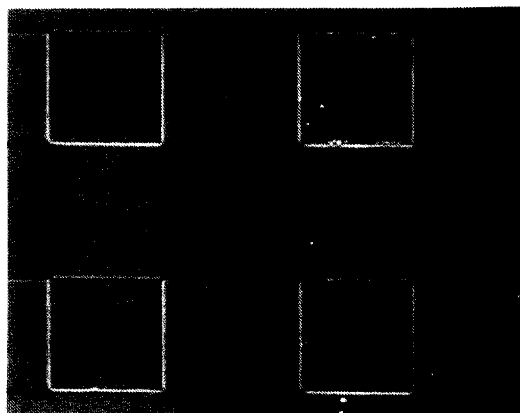

Fig. 1. SEM image of mesa patterned Si substrate. The width of mesa is 50 μm.

The dimension and qulity of patterned mesa structures were confirmed by scanning electron microscoped (SEM). One of those SEM images is shown in Fig. 1. This mesa structure has the width of 50 μm, largest width among the mesas used in this experiment. The sharply defined edge and flatness on mesa can be seen from the SEM image. For smaller mesas, the edge definition and flatness was not degraded.

These mesa patterned samples were cleaned again by Shiraki Si cleaning process [6] and introduced into the growth chamber. The sample was cleaned by outgssing at 550℃ for 25 sec was followed. The growth chamber contained both Si and Ge deposition source. The capacitance voltage measurement was performed *ex situ* in ambient. The C-V spectra were obtained by applying dc bias voltage modulated by high frequency (1 MHz) ac voltage and detecting the in-phase signal. In order to avoid the confusion by out-of-phase conductive component, the precise zero phase was maintained during measurement.

The UHV STM experiment was performed *in situ* after Ge overlayer formation. The samples used in STM experiment were made by Ge depostion on Si substrate at room temperature, followed by annealing at ~600℃. In this experiment,

Fig. 2. STM image of Ge/Si(100). The thickness of Ge is lower than the critical thickness. The image shows clear(2×1) reconstruction.

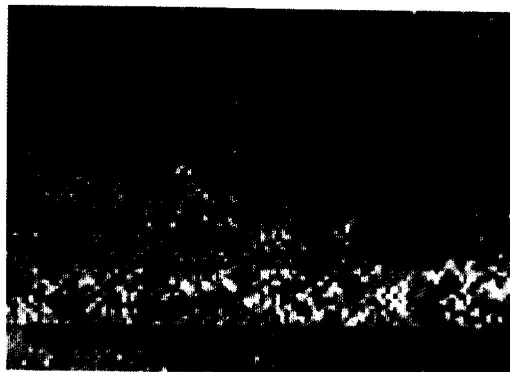

Fig. 3. STM image of Ge/Si(100). The thickness of Ge overlayer is highter than the critical thickness. The long-range-ordered (2×1) reconstruction shown in Fig. 2 is disappeared. For only small area, the (2×1) reconstructed domain can be shown. For most area of image, the disordered phase is distributed.

STM images were obtained for Ge coverages higher and lower than the critical thickness, respectively. For Ge coverage lower than the critical thickness, the surface morphology(shown in Fig. 2) showed the usual (2×1) reconstruction. The Ge overlayer was grown at the Si step edge preferentially. Especially, the preferential growth site was type 'B' step edge(having dimer row in upper terrace perpendicular to step) rather than type 'A' step edge (having dimer row in upper terrace parallel with step). This is consistent with the result reported previously [7]. For Ge overlayer thicker than the critical thickness, the long range ordered (2×1) reconstruction was disappeared, as shown in Fig. 3. Only in small area, the ordered phase could shown.

The samples for Raman, XPS, I-V and C-V meaurements were prepared by Ge and Si codepostition on Si substrate heated up to~600℃. After deposition, the annealing was followed in order to form a stochiometric layer. The fraction of Ge in Gesi layer was controlled by changing the growth rates of Ge and Si, respectively. And, for a few samples, the substrate heating temperature was changed. The thickness of Ge_xSi_{1-x} layer did not exceed~100Å.

Through XPS experiment, we confirmed the formation of Ge_xSi_{1-x} layer. But, the Ge_xSi_{1-x} layer was very thin, so only information on chemical composition was obtained. We performed micro Raman spectroscopy of Ge_xSi_{1-x} layer grown on plain Si substrate and mesa patterned Si substrate. For Ge_xSi_{1-x} layer grown on plain Si substrate, we observed the Si-Ge alloy peak at 410 cm^{-1}. This is the Si-Ge alloy peak position of fully strain-relaxed Ge_xSi_{1-x} layer. This fully strain-relaxed GeSi layer was prepared through thick Si, Ge co-deposition on Si substrate heated up to 750℃. The high temperature annealed thick Ge_xSi_{1-x} layer relaxes the lattice-mismatch induced strain by formation of misfit dislocation. For the sample prepared by Si, Ge co-deposition on messa patterned Si substrate heated up to 750℃ and post annealing at 750℃, micro Raman spectroscopy on mesa was performed. For this case, the position of Si-Ge alloy peak was at 413 cm^{-1}, rather lower than the position of fully relaxed layer. These results indicate the existence of a mechanism for strain relieving at mesa structure. For further investigation of function of mesa structure to strain relieving, it is necessary to perform the characterization of electronic states on the mesa patterned sample.

After the growth of GeSi layer on mesa patte-

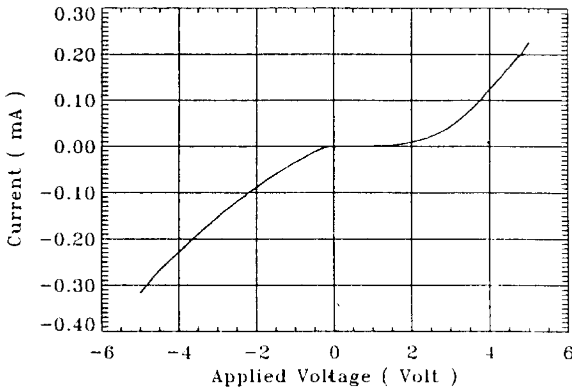

Fig. 4. I-V curve obtained at Ge_xSi_{1-x} layer grown on mesa patterned Si substrate.

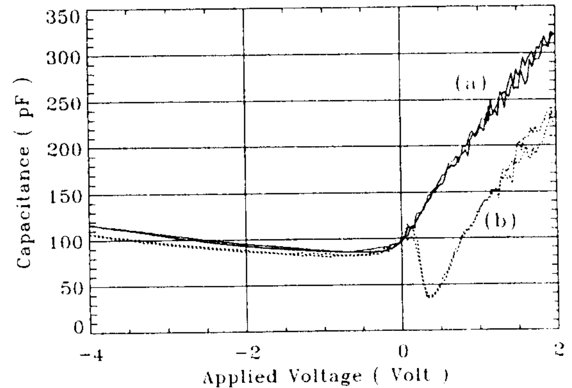

Fig. 5. C-V curve obtained at Ge_xSi_{1-x} layer grown on mesa patterned Si substrate. The data for forward and reverse direction of bias voltage ramp are shown together. (a) the data obtained at mid-point of mesa structure. (b) the data obtained at edge of mesa structure.

rned substrate, *ex situ* characterizations of the electronic structure of the samples were performed. In this experiment, I-V and C-V measurements were used. In I-V curve obtained on mesa structure, the anisotropy due to band offset can be shown. And, there is the break-down at 5~6 V. Occasionally, the change by trap state can be shown around 1 V. The typical I-V curve is shown in Fig. 4. In C-V curves, the curve obtained on mesa structure and the curve obtained on the boundary of mesa structure show quite different characteristics. The C-V curve obtained on mesa structure shows the usual heterostructure characteristics of different slopes for forward and reverse bias(shown in Fig. 5-(a)). However, the C-V curve obtained on the boundary of mesa structure shows another feature(shown in Fig. 5-(b). That is the state at~0.5 V. This state can be explained as the trap state due to misfit dislocation. From the existence of the trap state at boundary of mesa structure, we can deduce that the mesa edge plays a role as a sink of dislocation. Therefore, the mesa structure having a modest width can be used as the substrate for dislocation free strained layer.

We made the mesa structure with width ranging from submicron to 50 μm in order to investigate the mechanism of strain relieving as a function of substrate size. We found the strain relieving at Ge_xSi_{1-x} layer grown on mesa structure(finite size substrate), compared to Ge_xSi_{1-x} layer grown on plain Si substrate (infinite size substrate). And, the strain relief at mesa structure was related to the nucleation of strain dislocation at the edge of mesa structure.

Acknowledgement

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