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ON RECORD/PLAYBACK SIGNAL PROCESSING METHOD FOR DVCR WITH HIGHER AREAL DENSITY

***Sangmoon Lee, Youngjoon Choi, Yonghoo Sheen, Yunggil Kim**

Image & Media Lab., LG Electronics Inc. Ltd.
16 Woomyeon-dong, Seocho-gu, Seoul 137-140, Korea

Abstract-In digital video recording, higher areal density is strongly required for realizing digital VCRs. In order to accomplish higher areal density, we have implemented a system that has a narrow track pitch and can record data of about 30 Mbps(15 Mbps per channel) with the conventional S-VHS tapes.
After computer simulation using the characteristics of the experimental system, we have selected appropriate equalizer and detection method by taking into account performance and cost (including hardware complexity). As a result, the selected equalizer and detection schemes are cosine equalizer and integrated detection, respectively. The implemented system confirms reliable operation with a symbol error rate of less than 1×10^{-4}. In this paper, We will show the performance of the implemented system together with simulation results.

I. INTRODUCTION

Recently, the development of a digital VCR for consumer is strongly expected. If consumer digital VCRs are to have the same size cassette, the same recording time, and the same or better audio and video performances, as cpmpared to those of the present analog VCR, an extremly high recording density should be realized.

Generally, the higher areal recording density can be realized by improving either the linear packing density or track density[1].

In our experimental system, we choose to increase the recording density by reducing the track pitch.

This paper describes the record/playback signal processing method at the narrow track pitch with conventional S-VHS tapes for DVCR.

This paper is organized as follows. In section II, we survey technical specifications of DVCR to be implemented. In section III, we conduct simulation for the selection of an appropriate equalization and detection schemes for our DVCR to be implemented and discuss the simulation results. And in section IV, we conduct hardware simulation in order to evaluate the performance of the implemented equalizer and detection schemes and show the hardware simulation result. We also show the performance of actual system. In addition, we show the robustness of symbol error rate for off-track. this is very important for tape interchangeability. Finally, we have conclusions in section V.

II. TECHNICAL SPECIFICATIONS OF OUR EXPERIMENTAL DVCR

Specifications which we have studied for home-use digital VCR are shown in table 1.

Recording data rate(including ECC codes, SYNC data, etc) is about 30 Mbps. We have adopted the two channel recording scheme. So the one channel data rate is 15 Mbps. The drum diameter is 62 mm in order to realize a digital VCR using an conventional S-VHS tapes and the drum revolution is 1850 rpm.

Azimuth angle is set at ±15 degree for reducing the crosstalk interference due to guardbandless recording.

Recording time is 4 hours with 30 Mbps digital signals on the conventional analog S-VHS cassette. We have achieved this longer recording time by reducing the track pitch to 14.5μm and using a recording wavelength of 0.8μm, resulting in areal density of 5.84 μm^2/bit.

We have introduced an 8-10 modulation as channel coding. The power spectrum of 8-10 modulation is shown in fig. 1. The 8-10 modulation is suitable for magnetic recording, because it is able to reduce the runlength and the DC component of the recording data and make clock regeneration more reliable.

Table 1. Technical specifications of our experimental DVCR

Items	Specifications
Drum diameter	62 mm
Drum rotation speed	1850 rpm
Track pitch	14.5 μm
Relative velocity	6.038 m/sec
Minimum wavelength	0.805 μm
Recording bit rate	15 Mbps
Channel coding	8-10 Modulation
Linear packing density	63.1 Kbpi
Areal density	5.84 μm^2/bit
Areal packing density	110.5 $Mbpi^2$
Tape	S-VHS
Recording time	4 Hr.
Tape width	1/2 inch

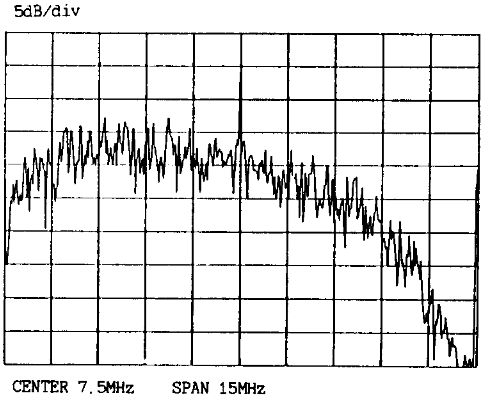

Fig. 1. Power spectrum of 8-10 modulated signal

III. SELECTION OF EQUALIZATION AND DETECTION SCHEMES

We have conducted simulations with different equalization and detection schemes in order to select an appropriate scheme for our experimental channel characteristics.

A. Channel model

The playback signal waveform due to a single transition in the write current is fundamental recording element in magnetic storage.

Assuming linear superposition holds for storage channels, the readback voltage signal, v(t), can be written as eq.(1).

$$v(t) = \frac{dw(t)}{dt} * h(t) + n(t) \tag{1}$$

Where w(t) is the write current and n(t) represents the effect of all distorting factors.

If w(t) is formed by NRZ modulation of the input bit stream, a_k, we have

$$w(t) = \sum_k a_k \Pi(t-kT), \qquad a_k \in \{-1, 1\} \tag{2}$$

where T is the symbol interval and

$$\Pi(t) = \begin{cases} 1 & \text{if } 0 \le t \le T \\ 0 & \text{otherwise.} \end{cases} \tag{3}$$

The output, therefore, corresponds to a differentiated and low pass filtered version of the current waveform applied to the write-head. From the above equations, it is straight forward to come up with a relation analogous to that of a pulse amplitude modulation(PAM) communication system:

$$v(t) = \sum_k a_k[\ h(t-kT) - h(t-kT-T)] + n(t) \tag{4}$$

The effective impulse response of the magnetic recording channel(also called dibit or pulse reponse), p(t), is, therefore,

$$p(t) = h(t) - h(t-T) \tag{5}$$

The above equation can also be written as:

$$v(t) = \sum_k b_k h(t-kT) + n(t) \tag{6}$$

where the transition sequence, b_k is given by

$$b_k = a_k - a_{k-1}, \qquad b_k \in \{-2, 0, 2\} \tag{7}$$

The overall recording process is then modeled by a digital filter with response (1-D) followed by the channel step response(also called isolated transition response), h(t).

The isolated transition response is generally approximated by the Lorentzian function given by:

$$h(t)=\frac{1}{pw_{50}}\cdot\frac{1}{1+(\frac{2t}{pw_{50}})^{2}} \qquad (8)$$

where pw_{50} denotes the pulse width at half of the maximum amplitude.

The extent of inter-symbol interference(ISI) is mainly determined by symbol density.

Symbol density D_s is defined as :

$$D_s=\frac{pw_{50}}{T_b} \qquad (9)$$

Where $T_b(=1/f_b)$ is the recording bit duration.

In simulation, we have used actual isolated transition response instead of the Lorentzian function. This actual isolated transition response is obtained by using digitizing oscilloscope from our actual DVCR. The measured isolated pulse is shown in fig. 2. The symbol density of our actual DVCR is calculated by eq.(9) and then symbol density is about 1.9.

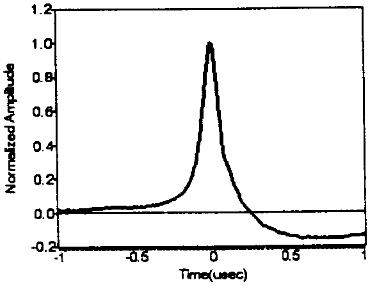

Fig. 2. Step response measured from actual DVCR

B. Simulation results

The relative performances of four different equalization and detection schemes are examined. The four schemes are PR(1) equalization(integrated detection), which is the reference case, PR(1,1) equalization with threshold detection, PR(1,0,-1) equalization with threshold detection and PR(1,0,-1) equalization with viterbi detection.

For the purpose of a fair evaluation, the number of taps of equalizer is identical for all schemes above. The number of taps of eqalizer is 11.

Fig. 3 shows the simulation result. The result is expressed as relative SNR loss(0 dB corresponds to $BER=1\times10^{-4}$ with PR(1) signal detection) in relation to BER.

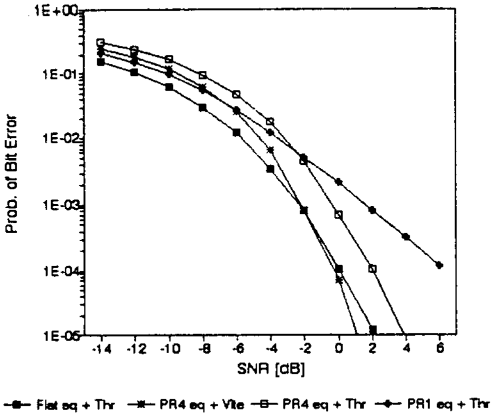

Fig. 3. Computer simulation results

From this simulation result, we can see that the performance of PR(1) is better than that of PR(1,1), PR(1,0,-1) with threshold detection. The result also shows that the performance of PR(1,0,-1) with viterbi detection is slightly better than that of PR(1) in high SNR.

According to our experiences, for $D_s > 2$, PR(1,0,-1) with viterbi detection is better than PR(1) with threshold detection in terms of BER.

Under the condition of BER 1×10^{-4}, the required SNR of PR(1,0,-1) with viterbi detection is lower by 0.3 dB than that of PR(1) with threshold detection.

Considering both this result and hardware complexity, we have selected PR(1) scheme.

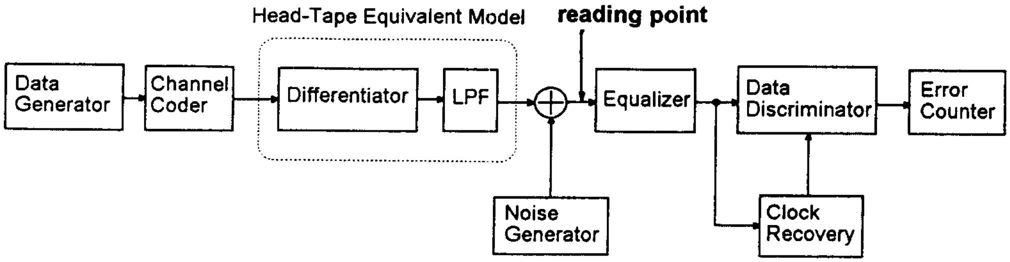

Fig. 4. Block diagram of system configuration for H/W simulation

IV. EXPERIMENTAL RESULTS

In order to implement the selected PR(1) scheme, we have designed and implemented a equalizer using cosine filter(called cosine equalizer).

Before the implemented scheme is installed on actual system, we have conducted hardware simulation to analyze the performance of the implemented equalization(including cosine equalizer and integration circuit)and detection schemes and to find the required SNR for particular target(1×10^{-4}). Fig. 4 shows system configuration for hardware simulation.

In hardware simulation, we have used the equivalent model of head-tape(which excludes mechanical effects). The equivalent model includes differentiator and low pass filter. And the noise is assumed to be additive white gaussian.

We have considered only one channel for hardware simulation. Therefore, ITI(Inter-Track Interference) and various factors(including spacing loss, system noise, drop-out, mechanical loss etc.) were not included in hardware simulation.

Fig. 5 shows relation between symbol error rate and SNR by hardware simulation. We assume that SNR is the ratio of a signal level(peak-to-peak value at the minimum recording wavelength) to a noise level (root- mean-squared value at a bandwidth of f_b, where f_b is bit rate) at reading point.

We have obtained symbol error rate of 1×10^{-4} at SNR 29dB. Therefore, in order to obtain symbol error rate of 1×10^{-4}, SNR at reading point of actual system must be greater than 29 dB. But this result didn't include various factors existing on actual system. So, system margin is required to satisfy a particular target. According to our experiences, system margin is required more than 3 dB. Therefore, the required SNR for obtaining symbol error rate of 1×10^{-4} is at least 32 dB.

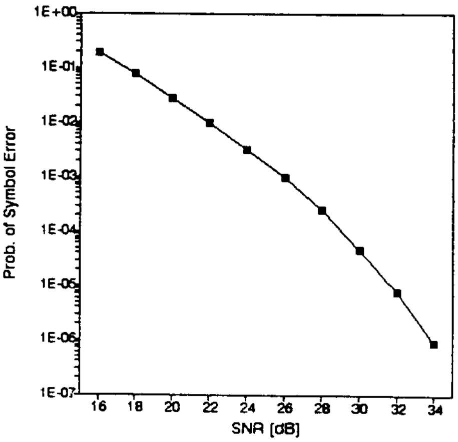

Fig. 5. Symbol error rate vs. SNR

The implemented schemes with this performance is installed and tested on actual system. Fig. 6 is power spectrum of reproduced signal at reading point of actual system. A SNR of 32.5 dB is obtained at this point. The symbol error rate of about 1×10^{-4} for actual system is obtained.

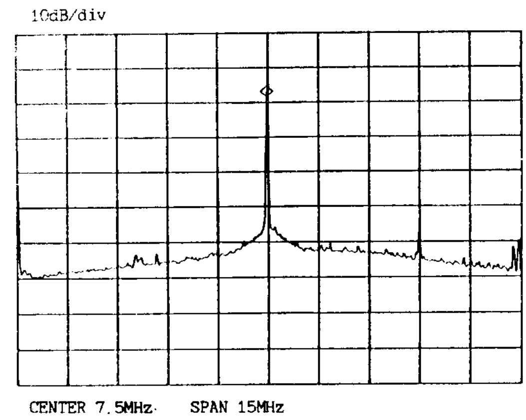

Fig. 6. Power spectrum of reproduced signal at reading point

We can see that the similarity of performance exists between the result of hardware simulation including system margin and that of actual system. Fig. 7 shows eye pattern of equalized signal.

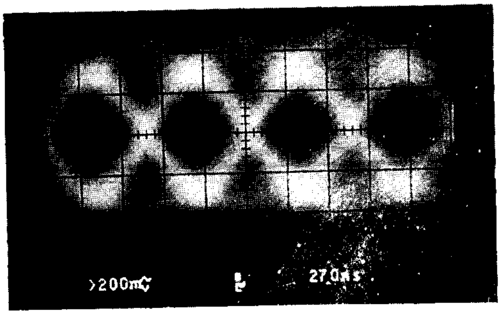

Fig. 7. Eye pattern of equalized signal

On the other hand, the robustness of symbol error rate to off-track is very important for tape interchangeability.

Fig. 8 shows the symbol error rate in terms of off-track. The symbol error rate of about 5 × 10^{-4} has been obtained in the off-track range of -5.7 μm to +5.7 μm. Considering error correction capability, we think that the symbol error rate of 5 × 10^{-4} is enough to provide a good picture quality.

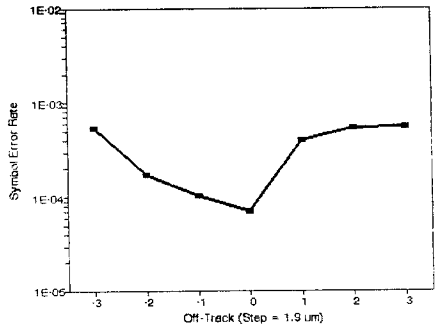

Fig. 8. Symbol error rate vs. Off-track

V. CONCLUSIONS

This paper has described a desirable signal processing method for realizing higher areal density for DVCR using conventional S-VHS tapes.

In order to realize higher areal density, we have reduced the track pitch to 14.5 μm.

Using computer simulation, we found out that an appropriate equalizer and detection scheme for our DVCR characteristics was PR(1) (integrated detection).

The symbol error rate of about 1×10^{-4} obtained in the actual system with conventional S-VHS tape. Also the symbol error rate of 5×10^{-4} has been obtained in the off-track range of -5.7 μm to +5.7 μm. As a result, we have seen a good possibility for the realization of home-use digital VCR from this study.

REFERENCES

[1] M. Kobayashi, et al., "Optimization of azimuth angle for some kinds of Media on digital VCRs," IEEE Trans. Magnetics, Vol. 27, No.6, Nov. 1991.
[2] S. Nakagawa, et al., "A Study on Detection Methods of NRZ Recording," IEEE Trans. on Magnetics, MAG-16, January, 1980.
[3] Roy D. Cideciyan, et al., " A PRML System for Digital Magnetic Recording," IEEE Journal on Selected Areas in Communications, Vol.10, No.1, January, 1992.
[4] M. Umemoto, et al., "Record and Playback Systems for 1.2Gbps HDTV Digital VTR," in Proc. 8th Int. Conf. Video, Audio & Data Rec., Birmingham, UK. April, 1990.