

Microfabrication of submicron-size hole for potential field emission and near field optical sensor applications

J. W. Lee, S. S. Choi, J. W. Kim, M. Y. Jung, and D. W. Kim

Dept. of Physics and Advanced Materials, College of Natural Science, Sun Moon University
(Received June 26, 1999)

전계방출 및 근접 광센서 응용을 위한 서브 마이크론 aperture의 제작

이주원 · 최성수 · 김종우 · 정미영 · 김대욱

선문대학교 자연과학대학 신소재과학과
(1999년 6월 26일 접수)

Abstract – The fabrication of the submicron size hole has been interesting due to the potential application of the near field optical sensor or liquid metal ion source. The 2 micron size dot array was photolithographically patterned. After formation of the V-groove shape by anisotropic KOH etching, dry oxidation at 1000°C for 600 minutes was followed. In this procedure, the orientation dependent oxide growth was performed to have an etch-mask for dry etching. The reactive ion etching by the inductively coupled plasma (ICP) system was performed in order to etch ~90 nm SiO₂ layer at the bottom of the V-groove and to etch the Si at the bottom. The negative ion energy would enhance the anisotropic etching by the Cl₂ gas. After etching, the remaining thickness of the oxide on the Si(111) surface was measured to be ~130 nm by scanning electron microscopy. The etched Si aperture can be used for NSOM sensor.

요 약 – Submicron aperture 제작 기술은 near field optical sensor 또는 liquid metal ion source에 응용될 수 있는 가능성으로 인해 흥미를 모으고 있다. 본 실험에서는 submicron aperture 제작에 대해 기술할 것이다. 먼저, 2 μm 크기의 dot array를 광학 리소그래피 방법으로 패터닝하였다. KOH 비등방성 식각 방법으로 V-groove 형을 만든 후, 1000°C에서 600분 동안 전식 산화 작업을 거쳤다. 이 산화 과정에서 결정 방향에 따라 산화율이 달라지게 되는데 Si(111) 면은 Si(100)면에 비해 산화율이 커서 두꺼운 산화막이 형성되며, 이 막은 연이은 전식식각 과정에서 etch-mask로 활용된다. Reactive ion etching은 ICP (Inductively Coupled Plasma) 장비를 사용하였으며, V-groove의 바닥에 형성된 90 nm 두께의 SiO₂와 그 아래의 Si를 식각하였다. 이 때, 기판에 걸린 negative bias는 Cl₂ RIE의 anisotropic etching 효과를 증대시키는 것 같았으며, SEM 촬영 결과 식각 후에 Si(111)면 위에는 약 130 nm 정도의 산화층이 잔류하고 있었다. 이렇게 형성된 Si aperture는 향후 NSOM sensor 등에 적용될 수 있을 것이다.

1. Introduction

There have been considerable interests in fabricating a submicron aperture for a near field optical sensor or liquid metal ion source [1-3]. The nanosize metal tip array can be fabricated using conventional semiconductor batch fabrication [4-6]. The etching of the Si using KOH solution will be anisotropic due to the different atomic density of the Si crystal surface. The etch ratio of the (111) Si surface to the (100) surface is greater

than a few hundreds. The intersection of the (111) surfaces will form eventually V-type groove or pyramidal shape at the bottom Si (100) surface [7-11]. The oxidation rate is also dependent upon the crystal plane. The higher packed Si (111) surface than the Si (100) surface will have a higher oxidation rate especially for the surface-reaction controlled region. The resultant thicker oxide on the Si(111) surface than Si(100) bottom surface during oxidation can be utilized as a mask oxide for submicron hole at the Si (100) bottom. We

utilized these phenomena for creating a submicron aperture. The submicron aperture array can be fabricated with anisotropic Si etching and orientation dependent oxidation followed by inductive coupled plasma etching. The silicon nitride film or the metal thin film can be deposited for its further application. The submicron or sub- 0.1 μm hole can be utilized for near field scanning optical sensor (NSOM) or liquid metal ion source.

2. Fabrication Procedures and Results

The p-type (5-15 Ωcm) 4 inch wafers were initially thermally oxidized to grow a 250 nm oxide layer. The 310 nm silicon nitride thin film was deposited on the SiO_2 layer by low pressure chemical vapor deposition (LPCVD) technique as shown in Fig. 1(a). The 2 micron dot array patterns were photo lithographed on the photoresist layer. The opening of $\text{Si}_3\text{N}_4/\text{SiO}_2$ double layer was fabricated with the reactive ion etcher (RIE). The RIE etching conditions for the Si_3N_4 layer and the SiO_2 layer were 600 watt RF power, a etching gas mixture of CHF_3 10 sccm, CF_4 10 sccm, and O_2 20 sccm, and plasma gas of Ar 10 sccm with an operating pressure 100 mTorr.

The 40 wt% KOH solutions will etch the Si substrate anisotropically with its etch rate $\sim 1 \mu\text{m}/\text{sec}$ at 80°C . The KOH etching at lower temperature will have slower etching speed.

The silicon etching at higher temperature than 80°C will result in the nonuniform etched surface. The V-groove formation by KOH etching was carried out as seen in Fig. 1. The width of the etched opening on the silicon surface (W_o) is related to etch depth (z) and the width of etched silicon surface at the bottom (W_s) given as follows:

$$W_s = W_o - 2z$$

In the case that the opening of the mask is small, the etched Si (111) surface will intersect each other and form V-groove. The oxide thicknesses grown at 1000°C with a dry O_2 ambient for 600 minutes are 330 nm at the Si (111) surface and ~ 90 nm oxide on the Si (100) bottom surface Fig. 2(a). The inductively coupled plasma etching was performed for submicron aperture

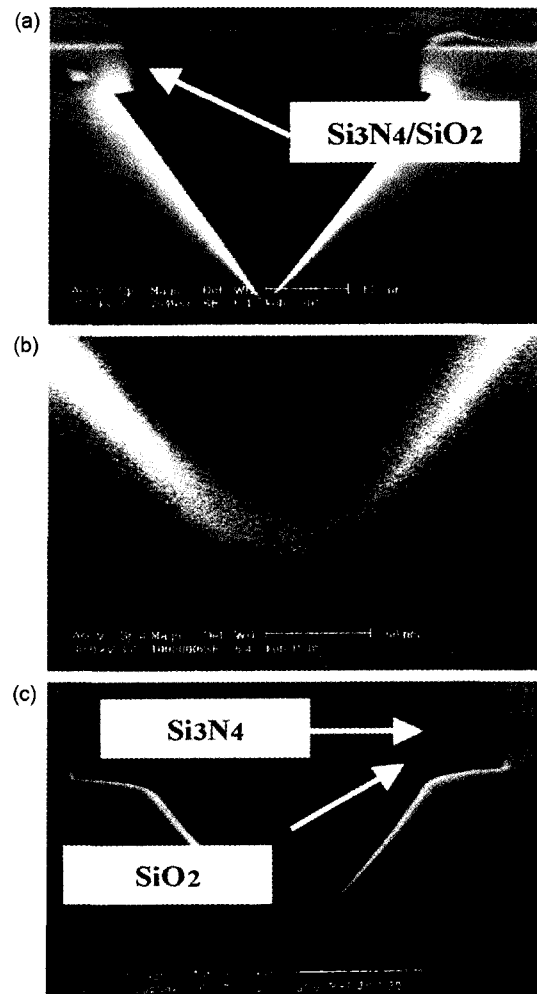


Fig. 1. The SEM micrographes of KOH etched Si-wafer: (a) After etching with a KOH 40 wt% solution, the etch-stop occurred and the V-type shape was formed. (b) an enlarged picture of 50 nm width of the bottom ($\times 1,000,000$) (c) After the KOH etching and the oxidation followed by the oxide etching, the oxide etch-mask just under the Si_3N_4 layer was partially etched.

at the bottom Fig. 2.(b).

The operating conditions were 100 watt RF power, 9 mtorr operating pressure, 40 sccm Cl_2 feed gas, and 5 minutes duration. The RF power to supply to the substrate was set to 200 W, and the bias voltage was measured to be ~ -450 eV. The negative bias on the substrate would create ion shower on the substrate and the ion-bombardments on the surface would enhance the surface desorption process during etching. The Cl_2

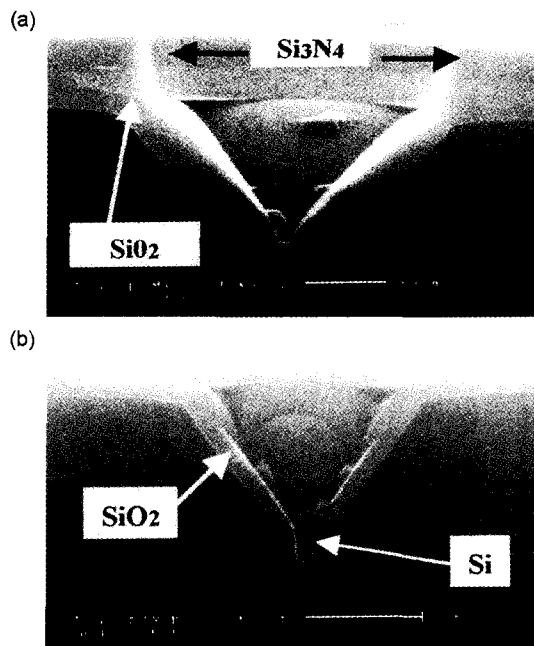


Fig. 2. The SEM micrographes present the orientation-dependent oxide thickness: (a) the thicknesses of the 54.7° (111) surface and the narrow bottom (100) surface are ~330 nm and 90 nm, respectively. (b) After ICP etching, bias-enhanced etching created a hole with ~0.1 μm width and ~400 nm depth in the Si at the bottom.

gas with Ar gas is also known to be very effective in providing anisotropic process. The etched hole of the Si was ~400 nm deep and ~100 nm wide Fig. 2(b).

3. Discussion and Conclusions

The submicron aperture on the silicon substrate was fabricated using various anisotropic processes. The LPCVD Si₃N₄ layer and the SiO₂ layer were used as an etch mask pattern. The wet chemical etching of KOH solution provides truncated pyramidal shape due to the anisotropic crystal plane dependent etching. After the

V-type formation, oxidation was performed and resulted in ~330 nm on the Si(111) surface and ~90 nm on the Si(100) surface due to fact that the higher silicon atom packing density on the Si (111) surface would provide thicker oxide from the surface reaction controlled mechanism. Using the biased inductively coupled plasma etching the oxide on the Si (100) was removed and the submicron hole on the Si (100) was created.

Acknowledgement

This work is supported by the Korean Ministry of Education (998-016-E00030).

References

- [1] R. C. Davis, C. C. Williams, P. Neuzil, *Appl. Phys. Lett.* **66**, 2309 (1995)
- [2] A. G. T. Ruiter, M. H. P. Moers, N. F. van Hulst, M. de Boer, *J. Vac. Sci. Technol.* **B14**, 5979 (1996)
- [3] C. Mihalcea, W. Scholz, S. Werner, S. Munster, E. Oesterschulze, R. Kassing, *Appl. Phys. Lett.* **68**(25), 3531 (1996).
- [4] I. Brodie, *Proceedings of The IEEE*, **82**(7), 1006 (1994).
- [5] C. A. Spindt, *Sur. Sci.* **266**, 145 (1992)
- [6] S. S. Choi, S. H. Lim, D. W. Kim, M. Y. Jung, H. Jeon, *J. Vac. Sci. Technol.* **B17**(2), 583 (1999).
- [7] K. Peterson, *Preceedings of The IEEE*, **70**(5), 420 (1982).
- [8] H. Seidel, L. Csepregi, A. Heuberger, H. Baumgartel, *J. Electrochem. Soc.* **137**(11), 3612 (1990).
- [9] G. T. A. Kovacs, N. I. Maluf, K. E. Peterson, *Proceedings of The IEEE*, **86**(8), 1536 (1998).
- [10] J. M. Bustillo, R. T. Howe, R. S. Miller, *Proceedings of The IEEE*, **86**(8), 1552 (1998).
- [11] R. Maboudian, R. T. Howa, *J. Vac. Sci. Technol.* **B15**, 1 (1999).