12-bit 파이프라인 BiCMOS를 사용한 A/D 변환기의 설계

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The Design of Analog-to-Digital Converter using 12-bit Pipeline BiCMOS

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Abstract

There is an increasing interest in high-performance A/D(Analog-to-Digital) converters for use in integrated analog and digital mixed processing systems. Pipeline A/D converter architectures coupled with BiCMOS process technology have the potential for realizing monolithic high-speed and high-accuracy A/D converters.

In this paper, the design of 12bit pipeline BiCMOS A/D converter presented. A BiCMOS operational amplifier and comparator suitable for use in the pipeline A/D converter. Test/simulation results of the circuit blocks and the converter system are presented. The main features is low distortion track-and-hold with 0-300MHz input bandwidth, and a proprietary 12bit multi-stage quantizer. Measured value is DNL = ±0.30LSB, INL=±0.52LSB, SNR=66dBFS and SFDR=74dBc at Fin=24.5MHz. Also Fabricated on 0.8um BiCMOS process.

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1. Introduction

There is an increasing interest in high -performance analog-to-digital converters for use in integrated analog and digital mixed processing systems. The realization of high -performance A/D converters typically has been limited to hybrid circuit technique. This paper is concerned with the design of 12bit pipelined BiCMOS A/D converter using chua's circuit[1,2,3]. The pipeline architecture offers the potential of high throughput rate at moderate circuit complexity and cost[4,5].

In this paper, the design of pipeline BiCMOS A/D converter using the Chua's circuit is presented. Chua's circuit uses a current source to force a current offset in the piecewise characteristics of a Chua diode. The Chua diode consists of a negative resistance converter, two ideal diodes, and a current source. A BiCMOS operational amplifier and comparator suitable for use in the pipeline A/D converter. Simulation results of the circuit blocks and the converter system are presented. The features differential analog inputs, a low distortion sample-and-hold with 0-300MHz input bandwidth, and a proprietary 12bit multi -stage quantizer. And Fabricated on 0.8um BiCMOS process.

## 2. Circuit description

2.1 Block diagram

The pipelining operation in the ADCs is very similar to the pipelining in digital applications. Figure 1 shows the pipelined BiCMOS block diagram used in this paper. The first stage of the ADC receives an input signal, processes it, and feeds the analog residue to the next stage. At the same time the digital output of the comparators are sent to a register block. Then the first stage accepts another input while the next stage starts processing this residue and so on. Although shown separately, the digital to analog converter, adder and the sample hold amplifier in the stage are designed as one amplifier block. Digital correction enables us to use fast but not very accurate comparators in an ADC without loosing any information.

Each stage must sample and hold the input signal for pipeline operation. The output of the stage must be amplified by a gain, which depends on the number of bits of the local ADC. Ideally this gain is an integer which is a power of 2. This simplifies the logic, and same voltage references can be used for each stage. If the same number of bits is used for each stage, this enables the designer to use the same layout for all stages. Pipeline ADCs are usually built in a CMOS process. This gives the industry a flexibility to integrate the ADC as a cell in a mixed mode integrated circuit. Because of its low cost, and low power properties, it is very advantageous to design analog circuits in a small geometry digital CMOS process. However it is harder to design accurate and fast analog circuits in digital CMOS compared to an analog process. Two main problems for analog circuits in digital CMOS process : 1. Low supply voltage, 2. Digital CMOS process does not need to support well matched double poly capacitors.

Most switched capacitor circuits use differential input differential output op-amps as the sample hold. Capacitors are used as feedback elements in the amplifier, so in order to achieve an accurate gain, the open loop gain of the op-amp must be high enough, and the

ratio of the feedback and sampling capacitors must be very accurate. In order to achieve high gain and high speed, most designs use cascode operational amplifiers.
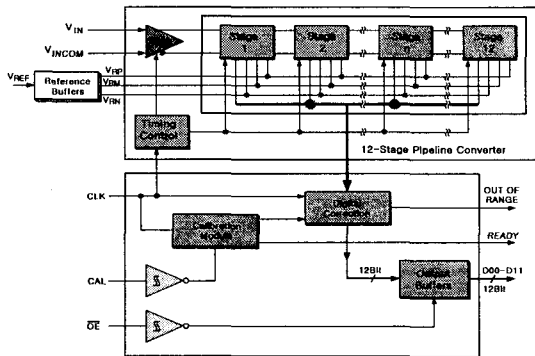
<Figure 1> Pipelined BiCMOS ADC block
diagram

2.2 Chua's circuit

Chua's circuit is a simple electronic network which exhibits a variety of bifurcation phenomena and attractors. The circuit consists of two capacitors, an inductor, a linear resistor, and a nonlinear resistor(called chua diode). The state equation for the circuit are as follows:

$$C1(dv_{c1}/dt) = G(v_{c2}-v_{c1}) - g(v_{c1}) \text{ --------}(1)$$
$$C2(dv_{c2}/dt) = G(v_{c1}-v_{c2}) + i_L \text{ ----------}(2)$$
$$L(di_L/dt) = -v_{c2} \text{ ------------------}(3)$$

Where G=1/R and g is a picewise-linear function defined by $g(v_R) = m_o v_R + \frac{1}{2}(m_1-m_o)$ $[|v_R+Bp| - |v_R-Bp|]$.

This relation is shown in graphically in Figure 2. The slopes in the inner and outer region are m_o and m_1 respectively; $\pm Bp$ denote breakpoints. The nonlinear resistor N_R is termed voltage-controlled because the current in the element is a function of the voltage across its terminals.
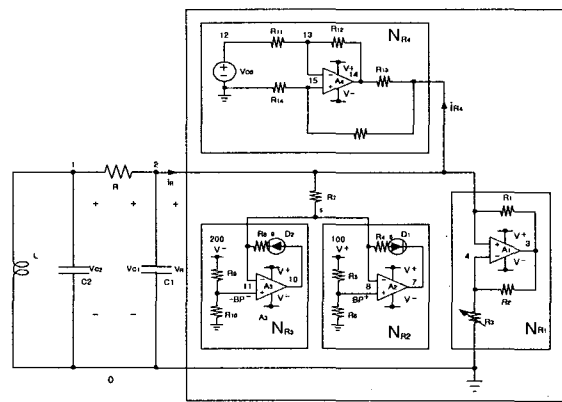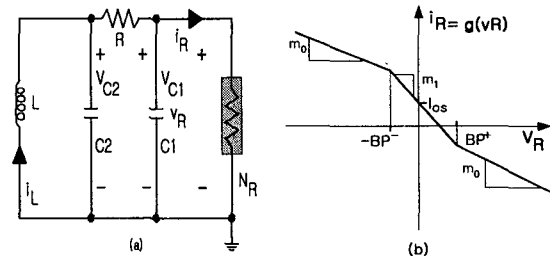
(c)

<Figure 2> (a)A current source *Ios* in parallel with the nonlinear resistor, (b)A current offset in the i-v characteristic, (c) Realization of Chua's circuit.

The i-v characteristic of a voltage-controlled nonlinear resistor may be offset along the i-axis by adding a current source in parallel with the element(Figure2(a),(b)). Realization of Chua's circuit using a current -offset Chua diode is shown in Figure 2(c). The desired nonlinear resistor characteristic is obtained by connecting in parallel a negative impedance converter N_{R1}, two ideal diodes(N_{R2} and N_{R3}), and a current source(N_{R4}) resistance. A negative resistance converter $N_{R1}(A_1,R_1,R_2,$ and R_3)is used to produce the underlying negative resistance. Connected in parallel with the negative impedance converter are two ideal diodes(A_2,R_4,D_1) and (A_3,R_8 ,D_2) with dc offsets

set by V+, R5, and R6, and V-, R9, and R10. Respectively. These connect a positive resistance R7 in parallel with the negative resistor NR1 whenever the voltage VR exceeds the breakpoints BP- and BP+ in magnitude. NR4 supplies the desired dc offset current Ios. This architecture allow one to control independently the slopes, breakpoints, and current offset of the Chua diode's i-v characteristic. In addition, several circuits be adjusted simultaneously by applying the same voltage Vos to each circuit.

2.3 Sample & Hold Amplifier

The S/H(Sample & Hold) amplifier is shown in Figure 3. This structure is similar to the multiply-by-two with $C_{m2}=0$ and $C_{m3}=0$. To simplify the analysis, assumptio- ns similar to the multiply-by-two concerning symmetry are used so that $C_h=C_{h1}=C_{h2}$. In addition, balanced op-amp halves are assumed. In a manner similar to the multiply-by-two, it can be shown that the governing difference equation is:

$$V_{od}(n)=V_{id}(n-2)+V_N(n)-V_N(n-1) ----------(4)$$

Thus, it is seen that the input is multiplied by one, as is desired for this S/H. The z-transform of equation (4) produces:

$$V_{od}(z)=V_{id}(z)z^{-2}+V_N(z)-V_N(1-z^{-1}) ---------(5)$$

Thus, CDS(Correlated Double Sampling) is performed with the same results as the multiply-by-two. The clock timing and charge injection issues for the S/H are analogues to the multiply-by-two.

PHI 1 controls : SH3, SH6
PHI 2 controls : SH1, SH4
PHI 3 controls : SH2, SH5
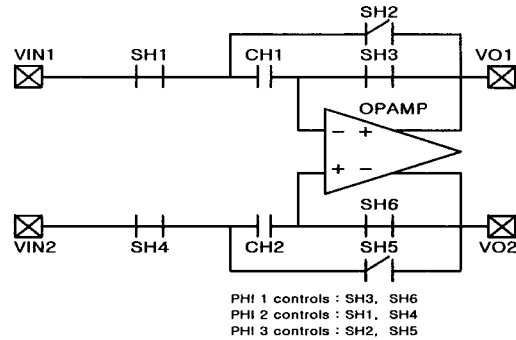
<Figure 3> S/H amplifier

2.4 BiCMOS circuit design

The focus in this paper is to present the design of the operational amplifier and comparator for use in the pipeline A/D converter. Ultimately, the performance of these circuits is related to device performance. In general, n-p-n devices offer superior gain and bandwidth over their p-n-p counters. As a result, the n-p-n devices is chosen whenever possible in the circuit design. The use of CMOS devices simplifies the design of basic logic circuits, such as inverters. Realization of switched capacitor circuits is possible using CMOS transmission gates. Active loads for n-p-n common emitter amplifiers can use either PMOS or p-n-p devices. As the p-n-p devices are not optimized BiCMOS process, PMOS active loads are used for such amplifiers. From a implementation point of view, this is not restrictive as most commercially BiCMOS process are designed for digital circuits and do not offer p-n-p devices.

Input differential pairs for the op-amp and comparator pre-amplifier utilize PMOS devices resulting in lower threshold voltage hysteresis[6] and lower $1/f$ noise power spectrum density compared to NMOS devices.

2.5 Operational Amplifier Design

The dynamic response of the op-amp is critical to the throughput and accuracy of the pipeline A/D converter. The basic topology of the op-amp is selected so that n-p-n devices available in BiCMOS can be best utilized. A folded-cascode topology can be used to achieve the high frequency response but op-amps with such topologies suffer from relatively low dc gain. A two-stage op-amp design can be satisfy the high frequency and high dc gain requirements. The two-stage op-amp is fully differential design. Fully differential systems have become popular recently for implementing a variety of integrated mixed signal processing functions. The main advantage of using such topologies is that common mode noise components can be effectively canceled. An added benefit is the extended dynamic range of differential signals compared to single-ended signals. Disadvantages of fully differential circuits frequently require common mode feedback circuits to set the common mode level. The common mode feedback is needed since two degree of freedom are present in differential signals, namely the differential mode and the common mode. The op-amp circuit is presented in Figure 4 and Figure 5.

The op-amp employs a PMOS differential pair in the first stage composed of device M_1 and M_2, shown in Figure 4. The PMOS devices provide a purely capacitive input impedance. Observing the right half portion of Figure 4, the input stage is actively loaded with transistor Q_7. The second stage is bipolar design consisting of common emitter amplifier Q_2 and cascade device Q_3. It can be shown that for a frequency compensated two-stage amplifier the non-dominant pole frequency is p_2

$\approx -G_{m2}/C_L$[7], where G_{m2} and C_L are the transconductance and load capacitances, respectively, of the second stage. The high transconductance of bipolar devices is used in the second stage to permit a high bandwidth by pushing the non-dominant pole out to a high frequency. A low impedance output buffer is not needed for this op-amp. The fully differential op-amp requires a common mode feedback loop to set the output common mode level. This op-amp uses a dynamic common mode feedback scheme for this purpose[8,9]. As the op-amp is a two-stage design, the common mode feedback circuit controls the effective first stage bias current to set the common mode levels of both the first and second stage outputs[10].
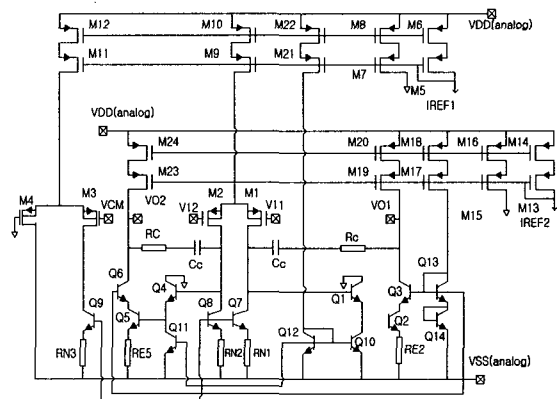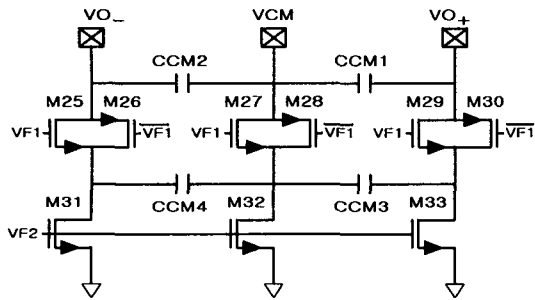

<Figure 4> BiCMOS operational amplifier main circuit

The input of the common mode amplifier is shown in Figure 5 as node V_{CM} at the gate of transistor M_3. An increase in this voltage causes each of the op-amp output voltage to decrease.

If a disturbance causes the output common mode level to increase, the common mode sense circuit will correspondingly increase

voltage V_{CM}. This cause the op-amp output common mode level to respond opposite to the disturbance, thus stabilizing the output common mode level. The common mode amplifier reference voltage is at node V_{CMR} connected to the gate of M_4. Since a differential input stage is used, the common mode feedback will attempt to drive the error voltage to zero. Thus, the common mode output level can be set by reference voltage V_{CMR}. It can be seen from Figure 4 that the common mode signal path is composed of the first and second stages of the differential amplifier in addition to the current mirror Q_7, Q_8, and Q_9.

<Figure 5> BiCMOS operational amplifier common mode feedback sense circuit
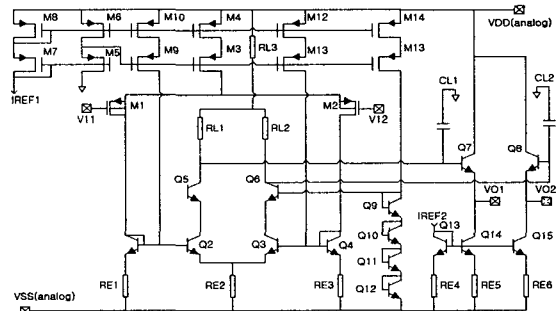
2.6 Comparator Pre-Amplifier Design

The primary function of the comparator pre-amplifier is to provide sufficient gain to overcome the input referred offset of the latch circuit. An open loop pre-amplifier circuit is chosen in order to meet the pipeline converter throughput and accuracy requirements. The open loop circuit is simpler compared to a feedback circuit but the open loop circuit involves a tradeoff between the d-c gain and dynamic range.

One possible pre-amplifier design uses a folded-cascode structure with a PMOS input

differential pair connected to a n-p-n or NMOS bipolar cascode. However, such a structure suffers from low d-c gain because of the low transconductance of the input PMOS differential pair. The low input transconductance can be compensated by using high output resistance current source in the output cascode.

The desired pre-amplifier is a two-stage, fully differential design using a PMOS differential pair as the first stage and a bipolar differential pair with cascode devices in the second stage. The Pre-amplifier is presented Figure 6. The substrates for NMOS and PMOS devices are implicitly connected to V_{SS} and V_{DD}, respectively, unless otherwise indicated. The p-well substrates for all n-p-n devices and poly-n+ capacitors are connected to V_{SS}.

The pre-amplifier employs a PMOS differential pair in the first stage composed of devices M_1 and M_2, shown in Figure 6. The first stage loads are composed essentially of resistors R_{E1} and R_{E2}. The second stage uses a bipolar differential pair composed of transistors Q_2 and Q_3. A novel scheme is used to establish the bias of the second stage.

<Figure 6> BiCMOS comparator pre-amplifier

The devices Q_1, Q_2, Q_3, and Q_4 comprise a current mirror using the first stage PMOS drains as reference currents thus establishing the bias for the second stage differential pair.

As a result, a separate source is not needed to establish bias for the second stage. A cascode structure composed of device Q_5 and Q_6 is used to extend the bandwidth of the pre-amplifier. Resistors R_{L1}, R_{L2} and R_{L3} are used as the loads for the second stage. A common mode feedback scheme is not needed for this fully differential pre-amplifier as the output common mode level is set by the bias current and the load resistors. Emitter followers Q_7 and Q_8 are used to buffer the second stage outputs.

2.7 Latch Design

The purpose of the latch is to amplify the pre-amplifier output to generate a digital output and then hold the state of this digital output. Regenerative designs have been shown to achieve a minimum power-delay product to achieve the necessary amplification[11]. The latch design incorporates a PMOS differential pair in order to provide a simple method to interface a differential input without connecting directly to the latch outputs. The latch is presented in Figure 7. The basic regenerative latch is composed of cross coupled inverters pairs M_3, M_4, and M_5, M_6. The transmission gate M_8, M_9 acts as a reset switch and device M_7 is the latch enable switch.

The operation of the circuit is straightforward. The circuit is in the reset mode when $\bar{\Phi}_1$=1 and Φ_2=1. When 2 = 0, a differential voltage is developed across the latch outputs depending on the PMOS differential input pair. By allowing sufficient time for the differential voltage across the latch outputs to exceed the cross coupled inverter pair offset, the latch outputs will swing to the correct state when subsequently

Φ_1=0. The time constant for the cross coupled inverter pair loop transmission is basically g_m/C_L where gm is the MOS device transconductance and C_L is the capacitance present at the output of an inverter. Since this time constant is on the order of several nanoseconds, the positive feedback will result in a full output voltage in several time constants if the differential input voltage reasonably exceeds the offset voltage.
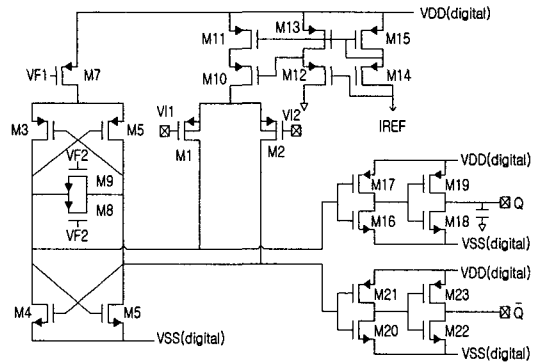
<Figure 7> Latch circuit

3. Simulation Results

Simulation results are first presented for the individual circuit blocks used to synthesize the pipeline A/D converter. The simulation results are then shown for the first two stages of the pipeline A/D converter. Basic circuit simulations were performed with HSPICE in SUN system.

3.1 BiCMOS Operational Amplifier

Table 1 gives a summary of the BiCMOS operational amplifier simulation results. When the effect of the mismatches is sought in the following simulations, only the op-amp mismatches are included. For these cases. 1%

mismatch for MOS device channel lengths and 0.1% mismatch for passive components are used.

<Table 1> BiCMOS operational amplifier simulation results

Parameter	Simulated Value
Differential mode d-c gain	114dB
Differential mode unity-gain frequency	150MHz
Differential mode phase margin	60°
Common mode d-c gain	114dB
Common mode unity-gain frequency	71MHz
Common mode phase margin	65°
CMRR	>81dB at 1 MHz
Positive PSRR	>85dB at 1 MHz
Negative PSRR	>81dB at 1 MHz
Input referred noise	11nV/√Hz
Slew rate	330V/usec
Capacitive loading per output	6pF
Step response max settling time(16-bit)	33ns
Differential output range power supply	12V
Power supply	±5
Power dissipation	82mW

3.2 BiCMOS Comparator Pre-Amplifier

Table 2 gives a summary of the BiCMOS comparator pre-amplifier simulation results. When the effect of mismatches is sought in the following simulations, only the pre-amplifier mismatches are included. For these cases, 1% mismatch for MOS device channel lengths and 0.1% mismatch for passive components are used.
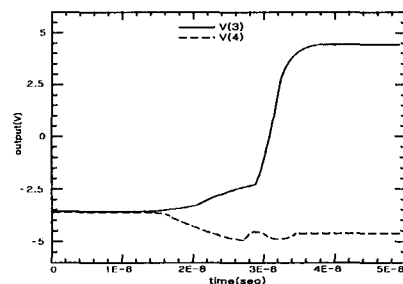
3.3 CMOS Latch

The simulation results for the latch are shown in Figure 8 and Figure 9. Referring to Figure 8, the cross coupled inverter outputs are denoted as $V(3)$ and $V(4)$. The latch is initially
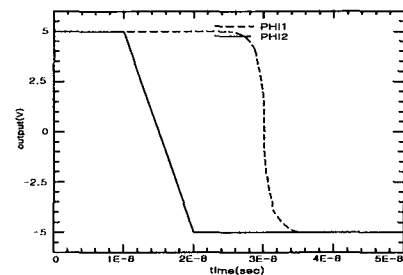
in the reset mode. When the reset switch is turned off, a voltage developed across $V(3)$ and $V(4)$ as a result of a large differential input. When the latch is energized, the outputs diverge and the latch will then be in the hold mode. The clocks for the latch are shown in Figure 9.

<Table 2> BiCMOS comparator preamplifier simulation results

Parameter	Simulated Value
d-c gain	33dB
-3dB bandwidth	38MHz
CMRR	>72dB at 1 MHz
Positive PSRR	>79dB at 1 MHz
Negative PSRR	>72dB at 1 MHz
Input referred noise	5nV/√Hz
Capacitive loading per output	5pF
Max offset cancel settling time(16-bit)	33ns
Differential output range	5V
Power supply	±5
Power dissipation	33mW

<Figure 8> Latch output

<Figure 9> Latch clock

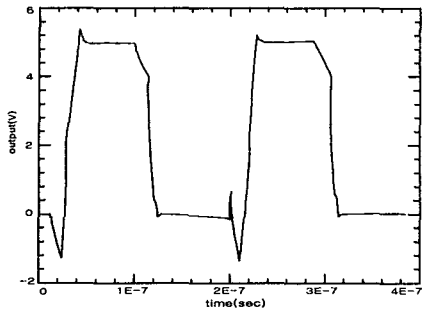## 3.4 BiCMOS Pipeline A/D Converter

The entire switched-capacitor BiCMOS pipelined A/D converter presents a formidable simulation task from a circuit level. The accuracy of the pipeline converter is determined primarily by the first few stages. As a result, placing focus on the first two stages provides most of the information that is sought from the simulation.

The simulation effort of fully differential systems depends on the choice of common mode feedback network model. The use of the complete switched-capacitor common mode feedback circuit can greatly extend the simulation time because the common mode level must first stabilize from the initial conditions. The simulation of the first two stages of the pipeline use op-amps employing a simplified common mode feedback network. The primary function of the common mode feedback is to sense the output common mode level. As a result, voltage controlled voltage sources provide an easy means in HSPICE to devise a common mode feedback sense network.
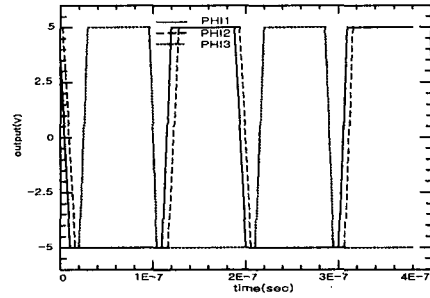
This section presents the simulation results of the first two stages in the pipeline A/D converter. The first stage employs a sample-and-hold switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch. The second stage employs a multiply-by-two switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch. Other support circuitry, such as digital inverters, are included in the simulation. In Figure 10, the analog output of the sample-and-hold is shown. Notice that the output alternately settles from 5 V and then to 0 V when reset. Figure 11 shows the analog

output for the multiply-by-two. Since the pipeline input is 5 V, the sample-and-hold out is 5 V. As a result, the MSB is set to 1. This causes the next stage to perform $V_{out} = 2V_{in} - V_{ref}/2$, following the reference non-restoring algorithm. Thus, the output of the multiply-by-two will be 5 V. As a result, the LSB is set to 1. Figures. 12 and Figure 13 show the digital outputs of the sample-and-hold and multiply-by-two stages, respectively. Detailed examination of the analog outputs reveals that this pipeline operates with 12-bit accuracy for a 10 V full scale. The clocks for the sample-and- hold analog system are shown in Figure 14. These clocks correctly sequence the switched-capacitor sample-and -hold function. The sample-and-hold digital system clocks are shown in Figure 15. These clocks correctly sequence the latch function in this stage. The clocks for the multiply-by-two analog system are shown in Figure 16. These clocks correctly sequence the switched -capacitor multiply-by-two function. The clock for the multiply-by-tow digital system are shown is Figure 17.
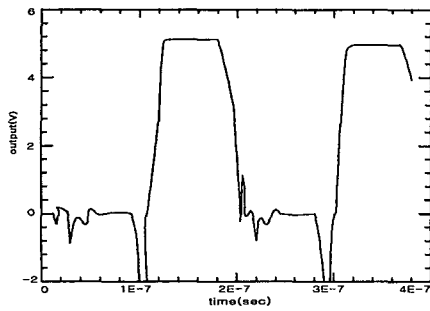
These clocks correctly sequence the latch function in this stage. The period of the clocks is 190ns. Thus, the throughput of this pipeline is about 5.2 MHz. The clock timing allocates 50 ns for op-amp and pre-amp settling. A substantial amount of time is needed for the clock waveform to slew. Additional time is allocated to assure non-overlapping clocks. Thus, the total overhead amounts to 90ns. Less conservative clock timing for 6.25 MHz throughput rate was successful in maintaining more than 12 bit of accuracy.
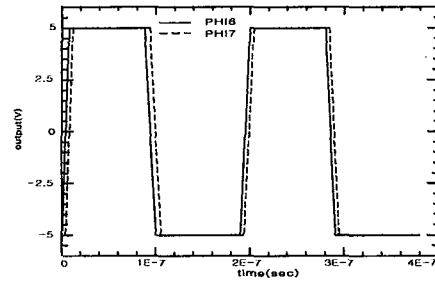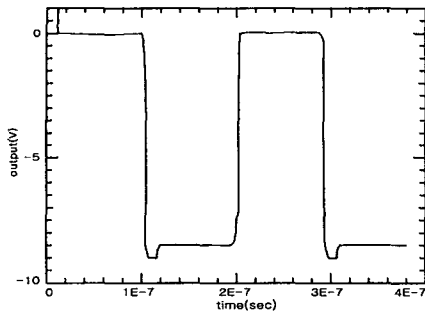
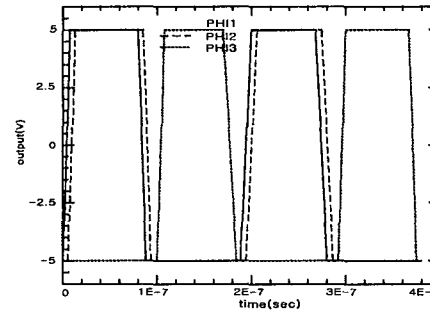<Figure 10> Sample-and-hold analog output

<Figure 11> Multiply-by-two analog output

<Figure 12> Sample-and-hold digital output

<Figure 13> Multiply-by-two digital output

<Figure 14> Sample-and-hold analog system clocks

<Figure 15> Sample-and-hold digital system clocks

<Figure 16> Multiply-by-two analog system clock

<Figure 17> Multiply-by-two digital system clock

And Figure 18, 19, 20 show the DC characteristics of DNL, ILL and SNR. DNL (Differential Non- Linearity) is measure of the maximum deviation from the ideal step size of 1 LSB. Measured DNL is ±0.30LSB(SPEC:± 0.65LSB). INL(Integral Non-Linearity) is a measure of the deviation of each individual code from a line drawn from negative full scale(1/2 LSB below the first code transition) through positive full scale. The deviation of any given code from this straight line is measured from the center of that code value. Measured INL is ±0.52LSB(SPEC:±1.15LSB).
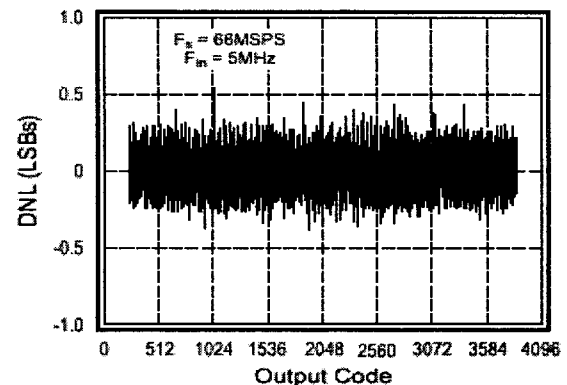
Finally, SNR(Signal to Noise Ratio) is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency. And SFDR(Spurious Free Dynamic Range) is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum. Measured SNR is 66dBFS at Fin=24.5MHz, and SFDR is 74dBc at Fin=24.5MHz. And fabricated final chip top view is represented as shown in Figure 21.
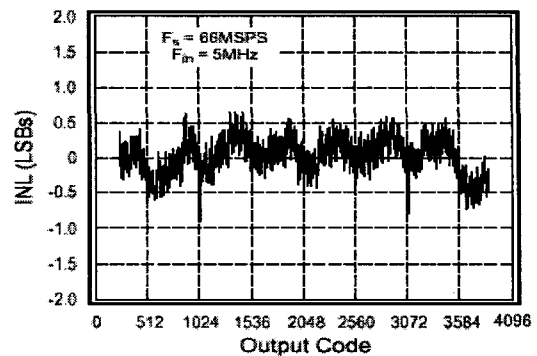
4. Conclusion

In this paper, the design of 12-bit pipeline BiCMOS A/D converter is presented. The operational amplifier design has emphasized

dynamic response as this circuit primarily determines the throughput of the pipeline A/D converter. A novel comparator pre-amplifier design used in an open loop offset cancelled comparator has been presented. Simulations have indicated a pipeline throughput of greater than 5 MHz for a 10 V full scale. A high frequency, fully differential BiCMOS operational

amplifier has been designed, fabricated and tested. Measured DNL = ±0.30LSB, INL=± 0.52LSB, SNR=66dBFS at Fin=24.5MHz, and SFDR=74dBc at Fin=24.5MHz. The performance measures indicate that this BiCMOS op-amp is suitable for high- performance applications.
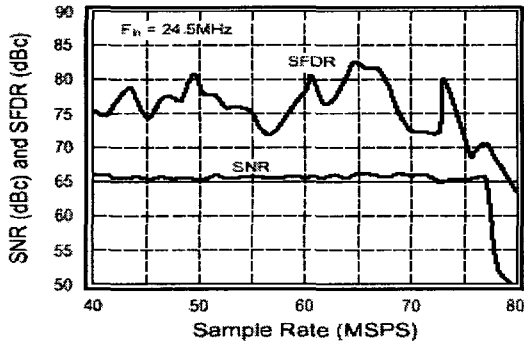
The design of the pipelined BiCMOS A/D converter can be optimized with simulation at the circuit and system level. Incorporating calibration schemes with pipeline architectures has the potential for realizing monolithic high-speed and high-accuracy A/D converters. This ADC can be used in high definition video, digital communication and cellular base -stations.
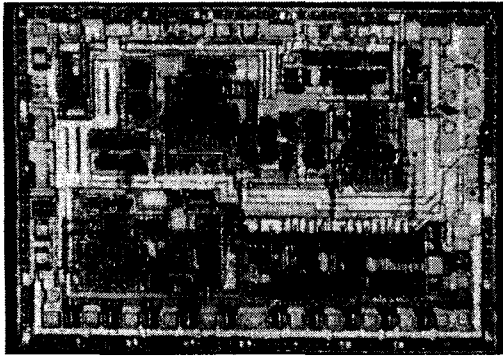

<Figure 18> Differential Non-linearity

<Figure 19> Integral Non-linearity

<Figure 20> SNR and SFDR vs sample rate

<Figure 21> Fabricated final chip top view

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