Micromachined Low-Loss Low-Dispersion Elevated CPW for High-Speed Interconnects

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Abstract

In this paper, 10 μ m-elevated MEMS CPWs on various substrates are presented. Effective dielectric constants of elevated CPW(ECPW) on polyimide-loaded silicon or alumina substrate are examined and characteristic impedances are also computed versus elevation height. Dispersive property of ECPW and its electromagnetic field distributions are studied through 3-D FDTD algorithm for optimum design. Attenuation of ECPW is measured with TRL calibration procedure and revealed about 3.2 dB lower than that of conventional CPW on the same low-resistivity silicon at 40 GHz. ECPW on polyimide-loaded silicon with overlapped configuration reveals 0.2 dB/mm. Especially, alumina substrate imposes better attenuation than silicon.

Key words : Elevated CPW, Low Loss, Low Dispersive, High-Speed Transmission Line

Ⅰ. Introduction

As the clock frequency in high-speed digital circuits and computers reaches a few giga-hertz regime, low-loss and low-dispersion signal transmission line is necessary. However, the performance of conventional transmission lines such as CPW or microstrip line implemented in CMOS compatible processing is limited to support high clock frequency signal and thereby exhibits quite dispersive and lossy characteristics. Various ways have been reported to improve the characteristics of conventional transmission lines. The method of removing the silicon substrate in the vicinity of the metal could lead to fabrication issues on mess production[1],[2]. Transmission lines with polyimide layer are presented by showing measured results[3]~[6]. High-resistivity silicon (HRS) revealed low RF signal leakage similar to GaAs substrate[7], however, HRS wafer is not cost- effective and further requires modification of standard CMOS process.

Recently, an elevated CPW geometry has been suggested without any measured data[8]. In this paper, various simulation results such as characteristic impedance, effective dielectric constant, electromagnetic field distributions, dispersive property, and signal velocity are uncovered with aid of a three dimensional finite-difference-time-domain method (3D-FDTD). Furthermore, measured total losses for transmission lines on three different substrates are presented for the performance comparison between conventional CPW and ECPW. In every case ECPWs reveal lower total loss than conventional CPW, and overlapped ECPW shows significant improvement of dispersion characteristics, signal velocity[9], as well as total loss in the range up to 40 GHz.

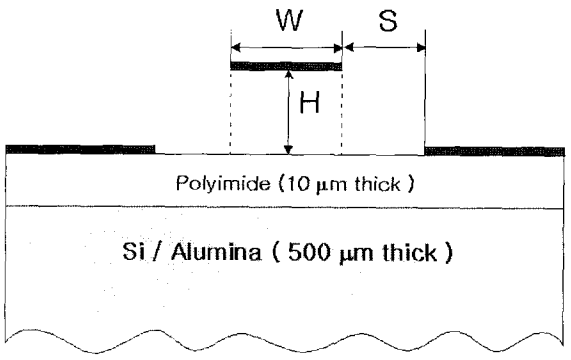

Fig. 1. Schematic of elevated coplanar waveguide on low-resistivity silicon or alumina substrate with 10 μm polyimide.

Ⅱ. Design and Fabrication

Conventional CPW supports quasi-TEM mode and is highly dispersive on CMOS grade silicon substrate due to air-dielectric interface and low resistivity, presenting limitations for the use on high-speed digital circuits. In this paper, the center signal line is 10 μm-elevated in the air to minimize the dispersive

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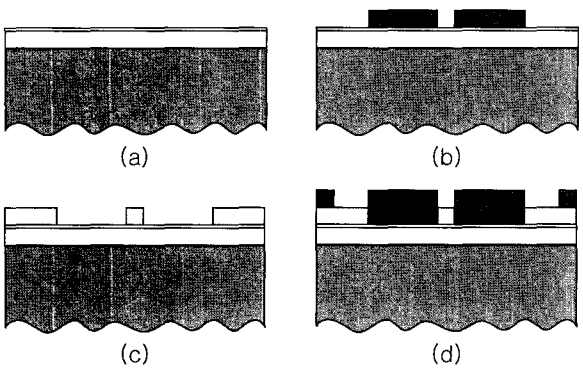
property as shown in Fig. 1. Important parameters to characte rize the ECPW performance are height of the elevated signal line(H), width(W), spacing(S) between the signal line and side ground planes, where negative value of S means the overlapped configuration. The ECPW lines having center conductor widths of 100 μm and 50 μm with 10 μm height are fabricated as shown in Fig. 2, where the area of supporters is 20×20 μm^2. Note that the height can be 40 μm to 60 μm without sacrificing mechanical stability. Since the distance between the supporters is 500 μm, the effect of the supporters can be neglected. Fabrication is relatively straightforward using standard liftoff processing and is compatible with standard CMOS process. In Fig. 3 fabrication procedure is described in detail. Polyimide with 10 μm thickness is coated on substrate materials. The three different substrate configurations such as a CMOS grade low-resistivity silicon, a polyimide-loaded standard silicon, and a polyimide-loaded alumina, are used. Conventional CPWs(i.e. H=0 μm) with spacings 20 μm, 60 μm, 100 μm are fabricated on each case. The 10 μm-ECPWs with spacing of -20 μm, 0 μm, 20 μm, 60 μm, to 100 μm, are fabricated on three different substrate configurations.

Fig. 2. SEM photograph of 10 μm-elevated coplanar waveguide.



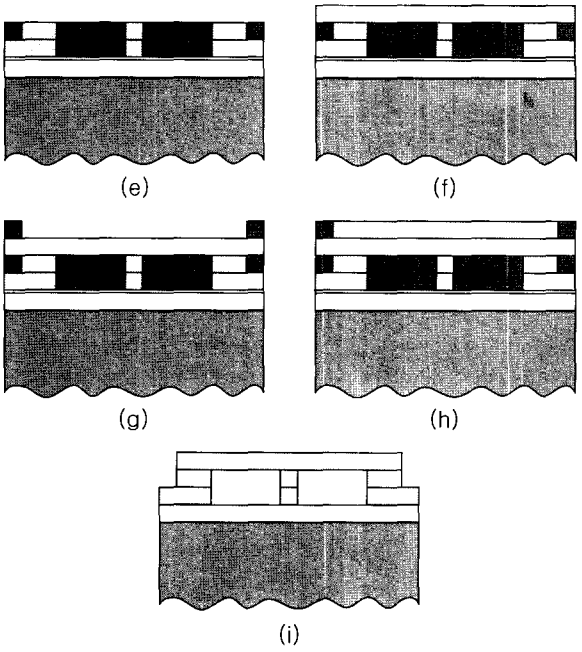


Fig. 3. Fabrication procedure.
(a) polyimide and first seed-layer coating
(b) PR coating and photo-lithography
(c) copper plating
(d) PR coating and photo-lithography
(e) copper plating
(f) second seed-layer coating
(g) PR coating and photo-lithography
(h) copper plating
(i) first and second seed-layer etching

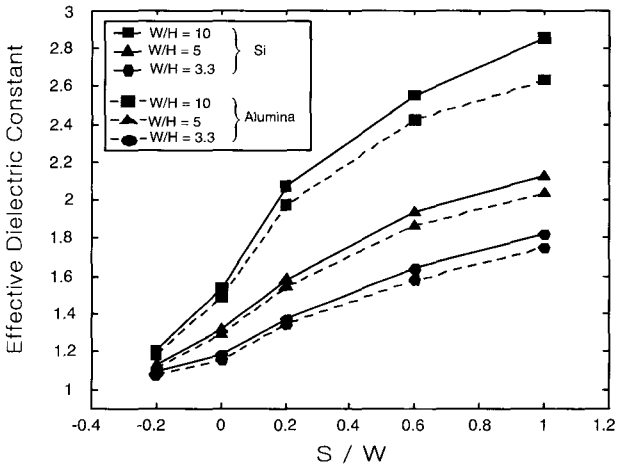


Fig. 4. Effective dielectric constant for polyimide-loaded silicon (ε_r = 11.9) or alumina (ε_r = 9.5).

Ⅲ. Theoretical Analysis

Yee's algorithm-based 3D-FDTD is used to analyze the cha-

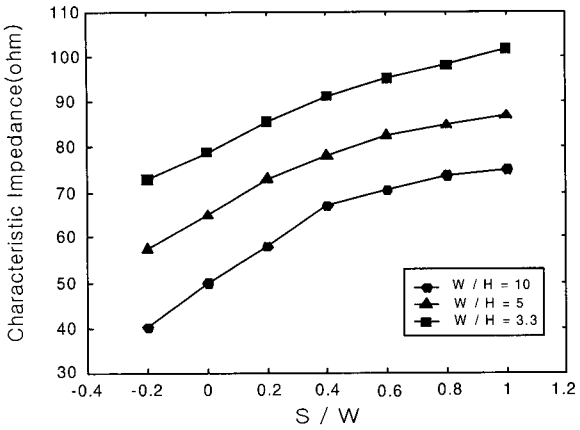


Fig. 5. Characteristic impedance for various geometry of ployimide-loaded silicon.

racteristics of the designed ECPW. Metal thickness is not considered in simulation. When signal line is elevated in the air, effective dielectric constant can be interpreted as the dielectric constant of a homogeneous medium that replaces the air and below multi-layer dielectric regions. For highly elevated geometry, very low effective dielectric constant close to 1 could be obtained for both silicon and alumina cases as shown in Fig. 4. Since signal velocity is inversely proportional to the square root of ε_{eff} high speed characteristic can be achieved by elevating center strip. ECPWs with negative S reveal minimum substrate dependency. As S increases ε_{eff} for alumina is much less than that of Si.

Various characteristic impedances ranging from 40 to 100 ohm are demonstrated with geometrical parameters W/H and S/W as shown in Fig. 5. As S and H increases Z_0 increases when W is fixed. Therefore high Z_0 can be acquired by elevating center strip for a fixed S and W without narrowing the center strip width. The transverse electromagnetic field distributions of a z-directed signal are shown in Fig. 6. Each contour line shows that the equipotential electric field and arrows represent the direction of the electric field vector and the length of arrow is the magnitude of the electric field. As shown in Fig. 6 (a), the fields of conventional CPW are distributed not only in the air but also in silicon substrate. However, the electric fields of ECPW are largely concentrated in the air region, especially in the vicinity metal edges as clearly shown in Fig. 6 (b) and (c). Note that most of electric fields are in the vicinity of air and polyimide in the case of $S=-20\,\mu$m. It means that the overlapped ECPW line is nearly isolated from the lossy silicon substrate and exhibits low loss characteristic.

As shown in Fig. 7, it is interesting to observe that how the Gaussian-shaped pulse propagates along the transmission lines of various geometries. The propagating signal on the conventional CPW on 10 μm-polyimide-loaded silicon is highly distorted and

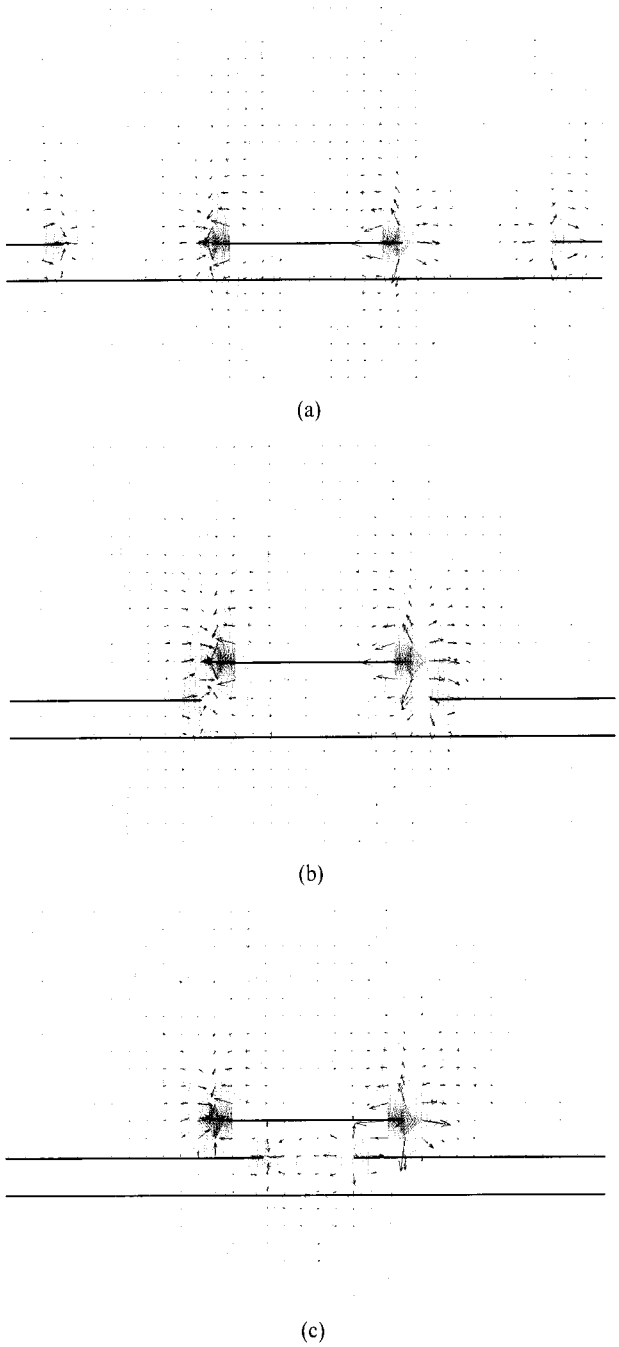


Fig. 6. Transverse electric field distribution on polyimide-loaded silicon.
(a) Conventional CPW(H=0 μm, S=100 μm)
(b) 10 μm-elevated CPW(H=10 μm, S=20 μm)
(c) 10 μm-elevated CPW(H=10 μm, S=$-$20 μm)

the signal velocity is significantly slower than that of the ECPW cases, thus it is not adequate for high speed circuits. It is clear that ECPW exhibits very low dispersion loss and supports high signal velocity as S varies from 100 μm to $-20\,\mu$m.

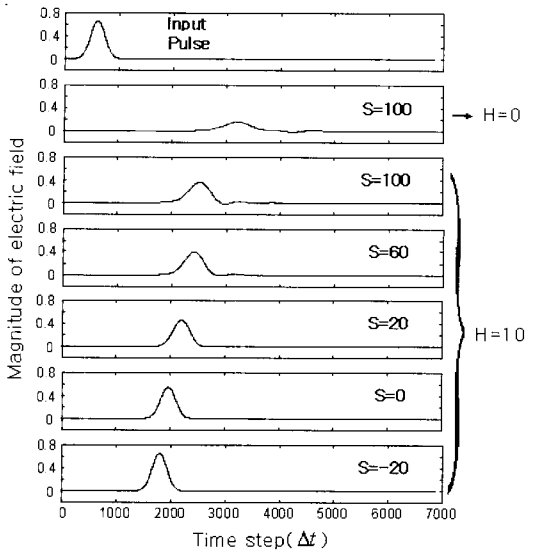


Fig. 7. Waveforms after 4.7 mm propagation for various geometries on 10 μm-polyimide-loaded silicon substrate.($\Delta t = 1.36 \times 10^{-14}$ sec.)

Pulses on the ECPW with S= −20 μm and S=0 μm propagate without any significant distortion and signal integrity is maintained very well. From the fact that the signal velocity of 20 μm -overlapped CPW is 1.8 times faster than that of conventional CPW, the ECPW structure can be accepted as a good candidate for high speed interconnects. Elevation height(H) is another critical parameter to characterize the performance of ECPW lines. Signal velocity for elevation heights is shown in Fig. 8. Signal velocity increases as elevation height increases at a fixed spacing. Also signal velocity decreases as spacing increases at a given height.

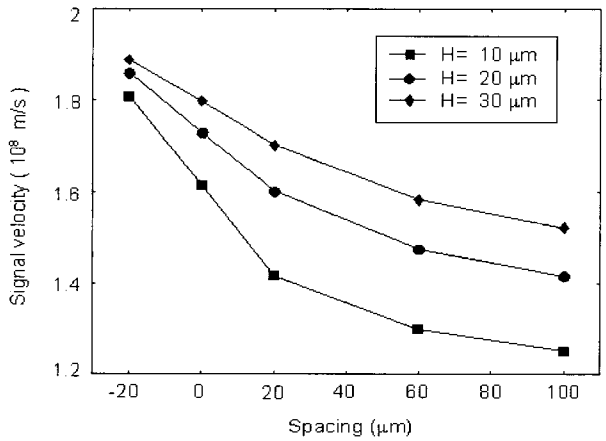
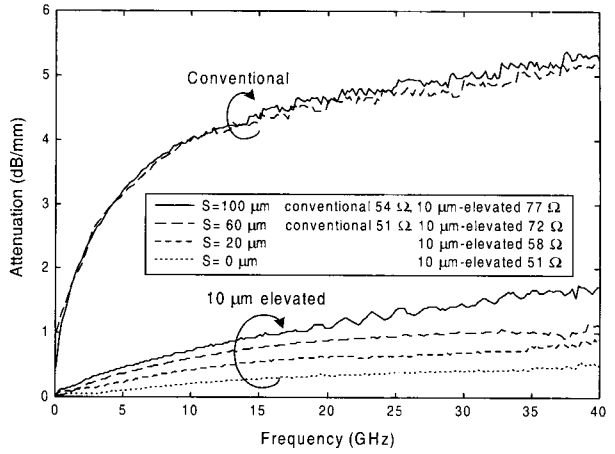
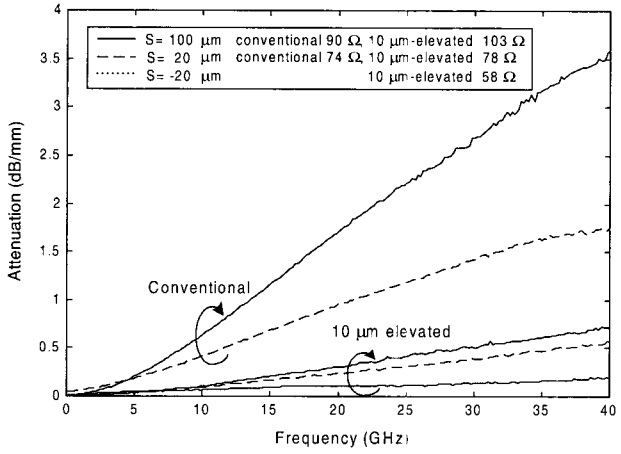


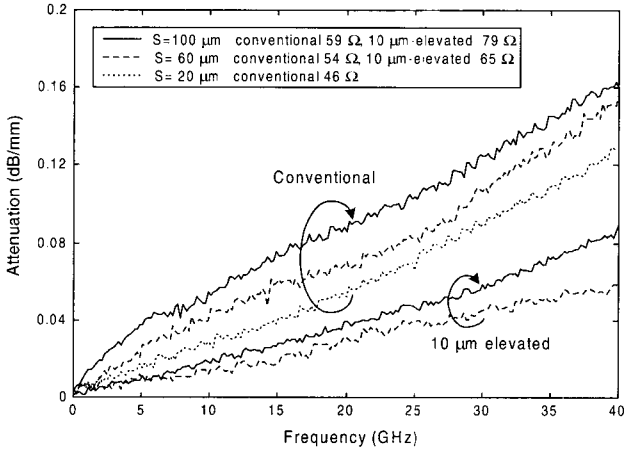
Fig. 8. Signal velocity along the ECPW line fabricated on standard low-resistivity silicon as a function of spacings and elevation heights.



(a)



(b)



(c)

Fig. 9. Measured attenuation for 10 μ m-elevated CPW on
(a) standard low-resistivity silicon(W=100 μm)
(b) polyimide-loaded silicon(W=50 μm)
(c) polyimide-loaded alumina(W=100 μm)

Ⅳ. Measurement

Attenuation of the fabricated ECPWs with three different substrates are measured using the Network Analyzer and GSG (Ground-Signal-Ground) high frequency coplanar probes. In order to minimize the parasitic effects, on-wafer TRL calibrations are carried out. Measured results are shown in Fig. 9 for three different cases. With the standard low- resistivity silicon the attenuation of the conventional CPW is 5.2 dB at 40 GHz and it is clear that these types of lines can not be used for high-speed circuits. The losses of the 10 μm -ECPWs are 2 dB lower than that of conventional one, and for the 10 μm-polyimide-loaded silicon the attenuation is significantly reduced at lower frequency region. Note that ECPW with $S=-20$ μm reveals the best performance of 0.2 dB below up to 40 GHz. As shown in Fig. 9 (c) the attenuation of ECPW on alumina substrate is about 0.16 dB below.

Ⅴ. Conclusion

10 μm-elevated CPWs are analyzed with 3D-FDTD and on-wafer measured results are presented. The effective dielectric constant, characteristic impedance, electromagnetic field distributions, propagating wave form, signal velocity, and measured total loss are well documented. The effect of elevation heights and spacings are thoroughly studied to characterize the performance of ECPWs. ECPWs on standard silicon have the effect of 3.2 dB attenuation reduction compared with conventional CPW. In the case of polyimide-loaded silicon, attenuation is much lower than that of standard silicon. Particularly, an ECPW with S=-20 μm reveals below 0.2 dB up to 40 GHz. The attenuation of 10 μm-polyimide-loaded alumina is below 0.16 dB for conventional case as well as elevated one. This indicates that low-loss alumina substrate imposes much better loss characteristics, even though low-resistivity silicon substrate can be used for high frequency application with center conductor elevation.

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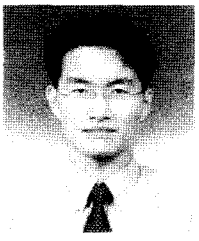

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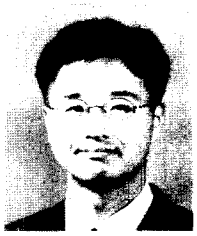
Jong-Gwan Yook



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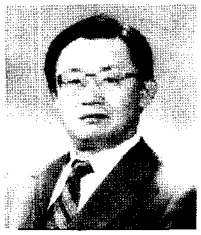

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