Multilayer Power Delivery Network Design for Reduction of EMI and SSN in High-Speed Microprocessor System

Seong-Geun Park[1] · Ji-Seong Kim[2] · Jong-Gwan Yook[1] · Han-Kyu Park[1]

Abstract

In this paper, a pre-layout design approach for high-speed microprocessor is proposed. For multilayer PCB stack up configuration as well as selection and placement of decoupling capacitors, an effective solution for reducing SSN and EMI is obtained by modeling and simulation of complete power distribution system. The system model includes VRM, decoupling capacitors, multiple power and ground planes for core voltage, vias, as well as microprocessor. Finally, the simulation results are verified by measurements data.

Key words : Multilayer PCB, Power-Ground Plane, Resonance, Simultaneous Switching Noise, EMI, Simulation, Decoupling Capacitor, Microprocessor, Target Impedance, Computer System Design

Ⅰ. Introduction

In today's modern computer system, as clock frequency reaches above 1 GHz and power supply voltage decreases, The importance of power/ground noise analysis has been greatly increased. The power/ground noise is one of the most difficult EM effects to be modeled due to the complexity of the power/ground distribution system (PDN). In chip package and multiple printed circuit board, power/ground planes with via holes constitute power distribution networks. Transient currents drawn by a large number of devices (core-logic, off-chip drivers) switching simultaneously can cause voltage fluctuations between power and ground planes, namely the simultaneous switching noise (SSN) or power/ground bounce. SSN will slow down the signals due to imperfect return path formed by the power/ground distribution system and cause logic error when it couples to quiet signal nets or disturb data in the latch. It may also introduce common mode noise in mixed analog and digital design or may increase radiation noise at resonant frequencies.

To avoid excessive SSN and to reduce electromagnetic interference (EMI) risk, the PDN must provide steady supply voltage within a specified range (typically ± 5 % or below) at desired frequency range in the presence of very large AC current demands. Consequently, it is necessary to carefully design complete PDN with properly located bulk and high frequency decoupling capacitors to control PDN impedances. Various works have been reported to model and simulate a pair of solid power/ground plane by means of several methods[1],[2]. This paper proposed a pre-layout physical design approach for power delivery systems through the analysis of the power/ground plane impedances and thus provides an optimal placement of decoupling capacitors in the multilayer PCB for high-speed processor systems. In the first step, power design strategy for microprocessor is planned to meet the power requirements, such as target impedance and noise budget. Secondly, the impedance characteristics of different PCB stack up strategies have been examined with SPICE, and finally the effective PDN design for microprocessor is obtained by simulation of complete structure, including voltage regulator module (VRM), bulk and decoupling capacitors, as well as microprocessor. The validation for the proposal approach is proved by comparing measured and simulated data.

Ⅱ. Design Methodology

2-1 Overall Design Procedure

The overall PDN design procedure for high-speed processor is illustrated in Fig. 1. From the given microprocessor specification, noise budget and target impedance can be obtained as follows:

$$Z_{\text{Target}} = \frac{(\text{PowerSupply Voltage}) \times (\text{AllowedRipple})}{\text{Maximum Current}} [\Omega]$$

To control the impedance of power/ground plane under the target impedance over the desired frequency range, power/ground plane is modeled with two dimensional lattice of transmission lines, and simulation and performed with decou-

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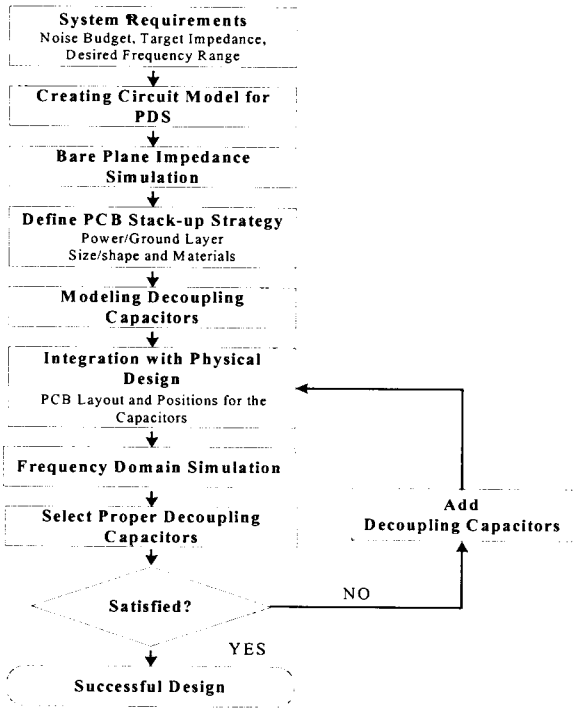


Fig. 1. PDN Design flow for microprocessor.

pling capacitors to find their optimal values and locations.

2-2 Circuit Modeling for Multilayer PCB

A pair of parallel planes can be modeled by a grid of transmission line equivalent circuits[3]. The low-frequency equivalent components of the planes can be derived from a quasi-static model. For a rectangular plane of dimension x and y, we first define the area u of a square unit cell as shown in Fig. 2, which should be equal to or less than 10 % of the shortest wavelength of interest. The cell size u is selected such that we have an integer N_x and N_y number of cells along the x and y direction, respectively. For every unit square of the plane with side dimensions of u, plane separation (dielectric height) of D, the static plane capacitance C and propagation delay along the edge TD can be computed. From the capacitance and delay, an equivalent characteristic impedance Z_{tline} and inductance L of the unit cell can be calculated as:

$$C = \varepsilon_0 \varepsilon_r \frac{u^2}{D}, \quad TD = \frac{u\sqrt{\varepsilon_r}}{c}$$

$$Z_{tline} = \frac{TD}{C} = \sqrt{\frac{L}{C}}, \quad L = Z_{tline} * TD = \mu_0 D$$

where c is the speed of light (3×10^8 m/s), μ_0 is the permeability of vaccum ($4\pi 10^{-7}$ H/m), and the DC resistance R_{dc} parameter is the resistance of both the power and ground

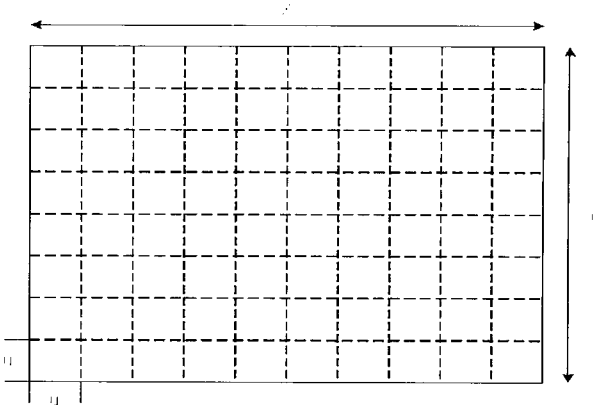


Fig. 2. Top view of a pair of power and ground planes that defines the transmission line.

planes for asteady DC current, where the planes are assumed to be uniform. The unit cells are replaced by four transmission lines along the edges of unit cells, each transmission line representing the same delay but only one quarter of the area, thus having an impedance of 4 Z_{tline}. Inside the equivalent grid, where the sides of unit cells touch, two transmission lines are connected in parallel, reducing the characteristic impedance to 2 Z_{tline}. Along the outer edges, the unit-cell transmission lines are standing alone. The parameters for the edge (Z_{edge}, TD_{edge}) and grid (Z_{grid}, TD_{grid}) transmission lines are given as:

$$Z_{edge} = \frac{4}{\sqrt{2}} Z_{tline}, \quad TD_{edge} = \frac{1}{\sqrt{2}} TD,$$

$$Z_{gird} = \frac{2}{\sqrt{2}} Z_{tline}, \; TD_{grid} = \frac{1}{\sqrt{2}} TD$$

The $\sqrt{2}$ correction factor is used to match the equivalent circuit's delay and impedance along the x and y axes. In addition, the lossy parameters should be considered for accurate modeling. The high frequency resistance R_{hf} accounts for skin effect both on top and bottom conductors, and the shunt conductance G represents the dielectric loss in the material between the planes. The frequency dependent parameters, such as R_{hf} and G, are taken into account by cadence PSPICE Analog Behavioral Model (ABM), which specifies the form of the S-domain transfer function. The lossy parameters of a unit cell can be computed as:

$$R_{dc} = \frac{1}{\sigma T}, R_{hf} = \sqrt{\frac{\omega\mu_0}{2\sigma}}, \quad G = \omega C \tan\delta$$

where T is conductor thickness and $\tan\delta$ is the loss tangent of the material, which is assumed to be frequency independent. The multilayer power plane is represented as a cascade of a power/ground plane pair connected by vias, while a pair of plane can be modeled as an array of SPICE circuit elements. As

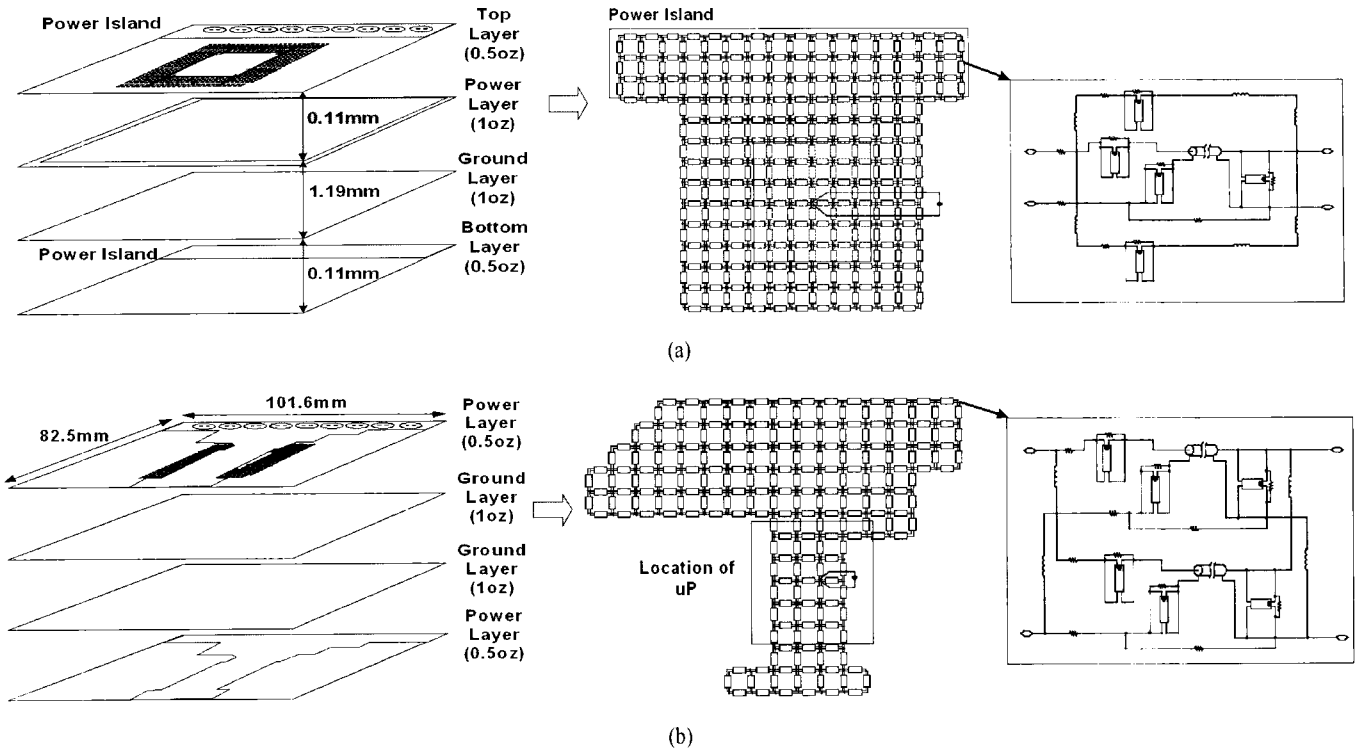


Fig. 3. (a) Conventional PCB stack up for processor power plane.
(b) Advanced PCB stack up for processor power plane.

shown in Fig. 3, the sub-circuits are composed of transmission lines with inductive vias, frequency independent DC resistor as well as frequency dependent resistor. It is also assumed that the number of vias is the same as nodes and the effect of mutual inductance is infinitesimally small. Therefore, viahole is represented as self- inductance and the equivalent inductance of vias can be compute as [4]:

$$L_{via} = \frac{\mu_0}{2\pi}\left[h \cdot \ln\left(\frac{h+\sqrt{r^2+h^2}}{r}\right) + \frac{3}{2}\left(r-\sqrt{r^2+h^2}\right)\right]$$

where h is the substrate thickness and r is the radius of the via cylinder.

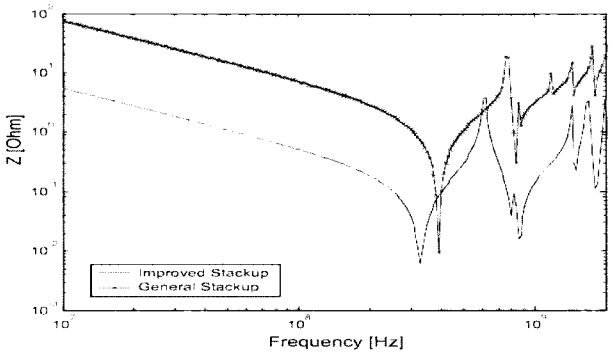
2-3 PCB Stack up Strategy

The parameters calculated above are used in circuit model to simulate power planes with SPICE. As shown in Fig. 3, two different of 4-layer PCB configurations for high-speed processor are considered to find optimum PCB stack up. The overall thickness of these boards is 1.57 mm and dielectric constant is 4.5. The conventional PCB stack up has been commonly used in 4-layer computer motherboard applications. It has a solid power/ground plane with power islands on top and bottom layers as shown in Fig. 3(a). In the other stack up, used in the high-end computer system applications today, the total stack up consists of two power planes on top and bottom layers, while two ground planes are placed inside as depicted in Fig. 3(b). Two different stack up geometries are simulated with 1 A AC current source placed at the center. Fig. 4. shows the magnitude of self impedance at the center and transfer impedance between center and edge. These plots show that the advanced PCB stack up geometry reveals much lower impedance.

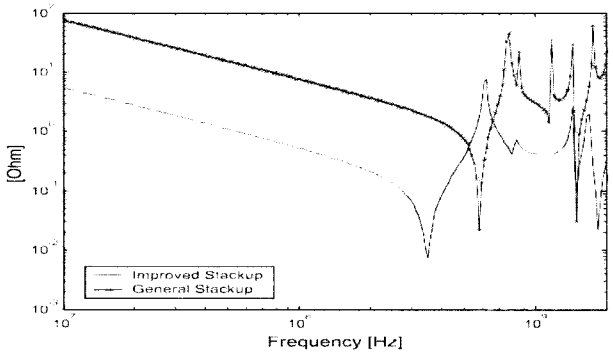
2-4 Decoupling Capacitor Strategy

Decoupling capacitors are modeled using series resistance, inductance, and capacitance (RLC) elements where R corresponds the ESR of the device, L represents the loop inductance of the pads, vias and also includes the inductance of the capacitor itself[5]. Capacitance gives a slope of 20 dB per decade on impedance versus frequency (Bode) plot, and inductance gives a 20 dB per decade slope. The curve bottoms out at impedance equivalent to the ESR value at the series resonant frequency. The minimum is at the frequency:

$$f_{\min} = \frac{1}{2\pi\sqrt{ESL \cdot Capacitance}}[\text{Hz}]$$



(a)



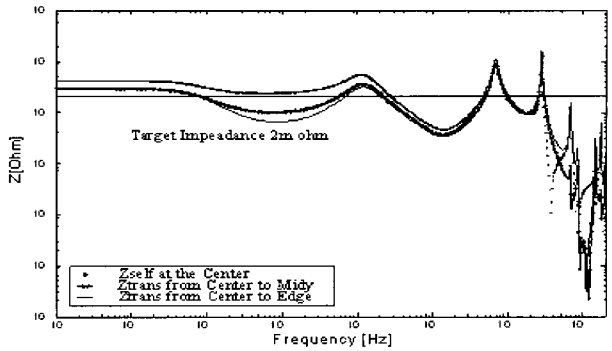
(b)

Fig. 4. (a) Simulated self impedance of bare plane.
(b) Simulated transfer impedance of bare plane.

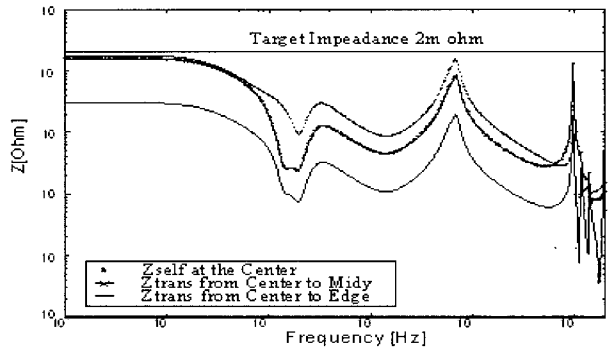
where f_{min} is the frequency of the low impedance dip associated with series resonance. Q or quality factor for an RLC circuit is equivalent to the reactive impedance divided by the resistance.

$$Q = \frac{Z}{R} = \frac{\sqrt{ESL/Capacitance}}{ESR}$$

Q is an indication of the sharpness of the resonance. The Q of the circuit is reduced by reducing L. The ratio of L/R is important. With a reduction in L, ESR can be reduced without increasing the Q of the circuit. High Q capacitors can lead to high impedance anti-resonant peaks if not managed properly. Fig. 5 shows simulated impedance characteristic of several different values of capacitance in parallel. Capacitors are placed in parallel until their parallel impedance meets the target impedance. Advantage is taken of resonance where ESR is lower than the impedance that can be reached by either the capacitive or inductive curve for that capacitor. This is key in minimizing the number of capacitors necessary to keep a PDS below target impedance. After obtain the proper value of capacitance by this method in a specified range, a cycle-by-cycle simulation is necessary find tune the optimal placement of decoupling capacitor with complete PDN system. The objective



(a)



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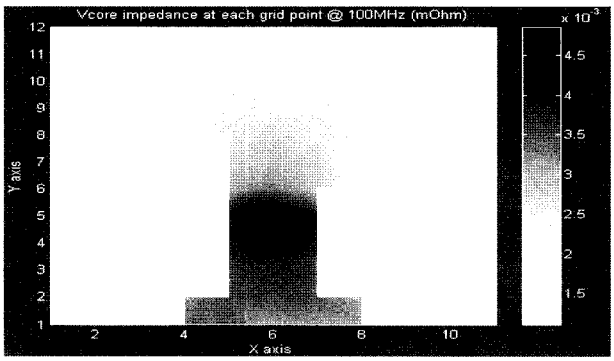


(c)

Fig. 5. (a) Impedance curves of PDN system without decoupling capacitor.
(b) Impedance curves of complete PDN system.
(c) Self impedance at each grid point at 100 MHz.

of decoupling capacitor is to minimize the impedance characteristics of the PDN in a specified frequency range. That will result in an acceptable amount of regulation noise.

2-5 Simulation of the Complete PDN System

In this section, simulations have been performed for the PDN system, which is consisted of the advanced stack up, power

Table 1. Decoupling capacitor models.

Type	ESR	ESL	No	Location
820 μF OSCON	6 mΩ	3.9 nH	4 ea	North side of the processor, close to power source (VRM)
2200 μF Al Electrolytic	11 mΩ	4.5 nH	6 ea	North side of the processor, close to power source (VRM)
1206 size, X7R, 10 μF	4 mΩ	1.19 nH	20 ea 6 ea	North side of the processor socket, mid point of the power plane South side of the processor, end point of the power plane
0805 size, X7R, 10 μF	4 mΩ	0.75 nH	18 ea	Inside the processor socket cavity

delivery model of microprocessor, linear model of VRM, and extended RLC model for decoupling capacitor. The processor requires 1.5 V core voltage, maximum current of 50 A, and consume 70 W, while the operating clock frequency is 2 GHz. The power delivery system should be designed to have its impedance less than or equal to the target impedance of 2 mΩ from DC up to 2 GHz. The processor and the linear VRM model are adapted from [6] and [7], respectively. The modeling parameters and locations of bulk and decoupling capacitor are described in Table.1. Fig. 5(a) shows the impedance characteristics of PDN with only bulk capacitors (820 μF and 2200 μF). The comparison between Fig. 5(a) and Fig. 5(b) reveals the effect of decoupling capacitors. Fig. 5(c) shows the self impedance at 400 MHz. The impedance plots follow the standing wave pattern over the planes. The transfer impedances are shown with the 1 A excitation at location corresponding to the peak on transfer impedance plot. The PDN impedance characteristics meet target impedance (2 mΩ) over frequency range from DC to 2 GHz. It is convincing that the VRM plays a key role to the low impedance characteristics up to 50 kHz, while the bulk capacitors up to 1 MHz and decoupling capacitors up to 30 MHz by supplying current. The impedance above 100 MHz is affected by the characteristics of power planes, and even further reduction is achieved by on chip capacitor in the microprocessor at high frequencies above 1 GHz. Note that the peak value of anti-resonance near 70 MHz is associated with impedance feature of ceramic capacitors and power plane.

Ⅲ. Measurement

For the validation of proposed pre-layout design approach, the physical PDN for high speed microprocessor is fabricated and tested. First, Bare board with the advanced PCB stack up geometry as shown in Fig. 3(b) was selected to correlate simulated and measured impedance. Self and transfer impedances were measured with HP8753 two port network analyzer at the center and edge of the test board as shown in Fig. 7(a) and (b). In the low and mid frequency range, the results are good agreement between simulated data and measured data. And the measured impedance is higher than the simulated result in high

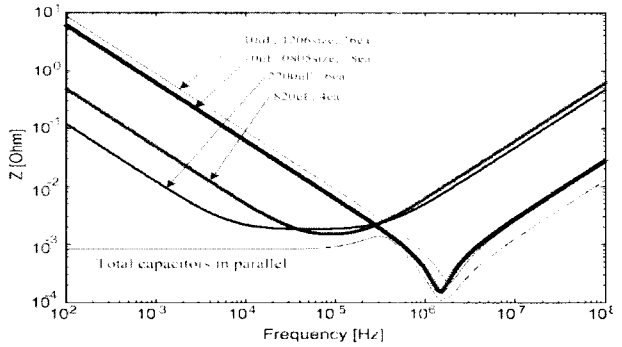
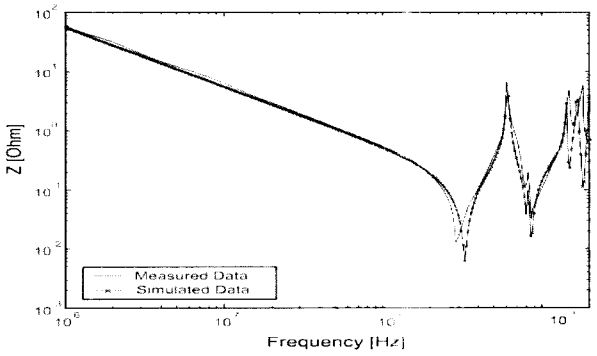
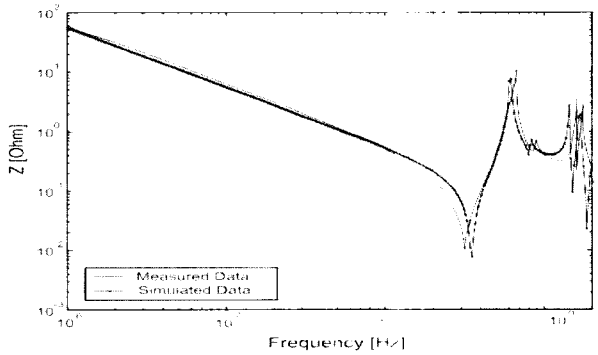


Fig. 6. Several values capacitors are placed in parallel without bare board.

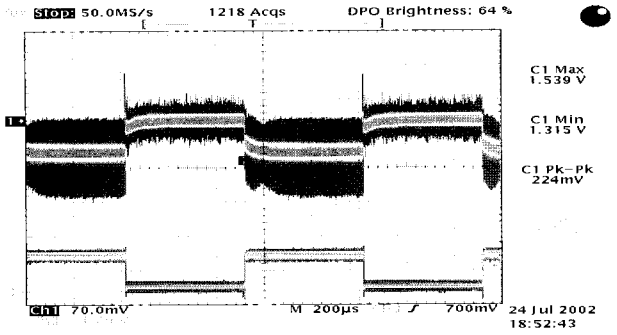


(a)

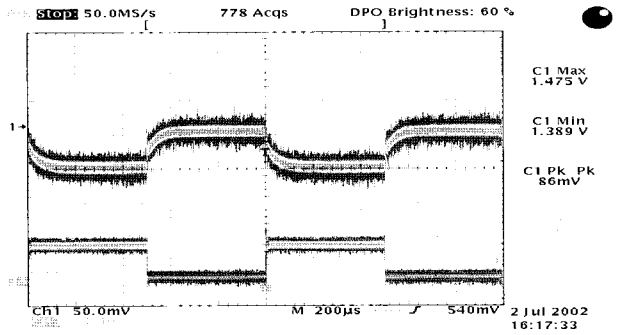


(b)

Fig. 7. (a) Measured and simulated self-impedance at the center.
(b) Measured and simulated transfer-impedance from the center to edge.



(a)



(b)

Fig. 8. (a) Measured transient response without decoupling capacitor.
(b) Measured transient response with decoupling capacitor.

frequency region. That is considered as capacitor pad and via effect of the test vehicle. Test environment and methodology are well described in [8]. To improve the measurement accuracy at low impedance readings, two-port S_{21}-based self-impedance measurement was used. The S_{21} parameter readings were converted to self and transfer impedance values by the approximate formula $Z = 25S_{21}$ [8]. The Fig. 7(a) and (b) reveals good agreements between simulated data and measurement data. Finally, for the time domain analysis, test board shown in Fig. 7 is built with the advanced PCB stack up geometry and decoupling capacitors are placed as simulated in the previous section. The peak-to-peak voltage noise in time domain is measured after supplying high slew rate transient current as shown in Fig. 6. The testing system is loaded with 50 A of current with slew rate of 200 A/μ s. The corresponding voltage requirements are 1.5 V, 1.327 V (173 mV_{p-p}) for V_{max} and V_{min} respectively, according to the electrical specification of the test system processor. The measured data show that the value and location of the decoupling capacitors are well optimized and the system satisfies with power delivery requirement.

Ⅳ. Conclusion

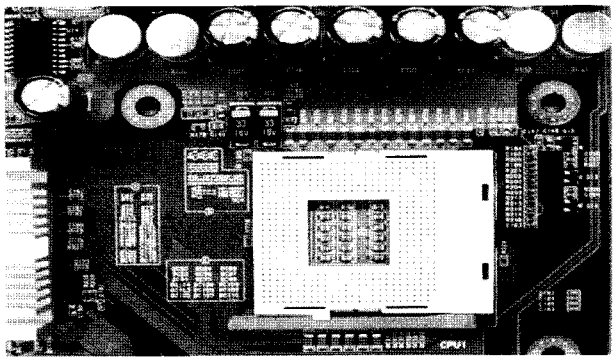


Fig. 9. Physical PDN for high speed microprocessor.

This paper presents a pre-layout design approach for power delivery systems of microprocessor. The modeling of the multilayer physical PCB stack up and simulation methodology of the complete PDN system are also proposed. The goal of the proposed approach is to guide optimal stack up as well as selection and placement of decoupling capacitors for modern high-speed processor system under the power delivery requirements over the desired frequency range. Finally, simulation results of the power plane are confirmed with the measured data of the test system. The proposed approach can be applied to design modern high-speed computer system without expensive time-consuming prototyping.

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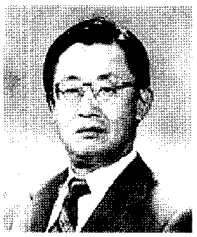

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