Analysis of EMI Problems in Split Power Distribution Network

Hwang-Yoon Shim[1] · Ji-Seong Kim[2] · Jong-Gwan Yook[1] · Han-Kyu Park[1]

Abstract

Signal integrity problems and their possible solutions are addressed in this paper for split power plane of high-speed digital systems. Stitching and decoupling capacitors are proved to be very effective for reducing signal noise, ground bounce as well as electromagnetic radiation from the split power plane. Simulations based on 3D-Finite Difference Time Domain (FDTD) method are utilized for the analysis of practical high frequency multi-layered PC main board

Key words : FDTD Method, Split Power Plane, EMI Problems, Stitching and Decoupling Capacitor

Ⅰ. Introduction

Today's personal computer has system clock operating at a few hundred MHz, and its knee frequency reaches a few giga-hertz regions ($F_{knee} = 0.5/T_r$) [1]. In modern high performance microprocessor design, multiple power and ground planes are indispensable elements due to the requirement of various power sources. However, the split reference plane causes serious signal integrity problem as well as electromagnetic (EM) radiation, affecting the performance of high-speed microprocessor circuit board. Spurious electromagnetic radiation occurs from the split power plane discontinuity, because currents are forced to flow around the slot and charges accumulate on its edges. As the current travels down the trace, the return current is induced on the reference plane. When signal reaches the gap, one portion of the reference current propagates across the gap via the gap capacitance, and the other portion is forced to travel around the gap or reflected backward. Both coupling and radiation caused by non-ideal return current path could lead to deteriorated signal integrity as well as electromagnetic compatibility problems in high-speed digital circuit. Works have been done to analyze noise tendency in this discontinuity model especially in signal distortion on transmission line[2]~[4].

This paper verifies the level of signal noise from different point of views such as scattering parameter, time domain noise distribution as well as EM radiation with and without placing the stitching/decoupling capacitors in small practical micrometer trace/slot structure.

Ⅱ. Design and Fabrication

For the characterization of the split power plane, practical 4-layer personal computer main board has been modeled with FDTD method as shown in Fig. 1. The microstrip line has 150 μm width and is crossing the 750 μm open slot printed on the FR4 substrate of $\varepsilon_r = 4.4$ and 125 μm thickness, the substrate between power and ground plane has 1,000 μm thickness. In stitching method, capacitor is placed between two power planes with different potentials, while in decoupling method, capacitor is located between the power and ground planes. These two methods are designed to provide well-established return current path to reference plane.

The signal line above the slot in the power plane is modeled as series inductor, and the decoupling or stitching capacitors are added near the slot to compensate signal noise due to the series

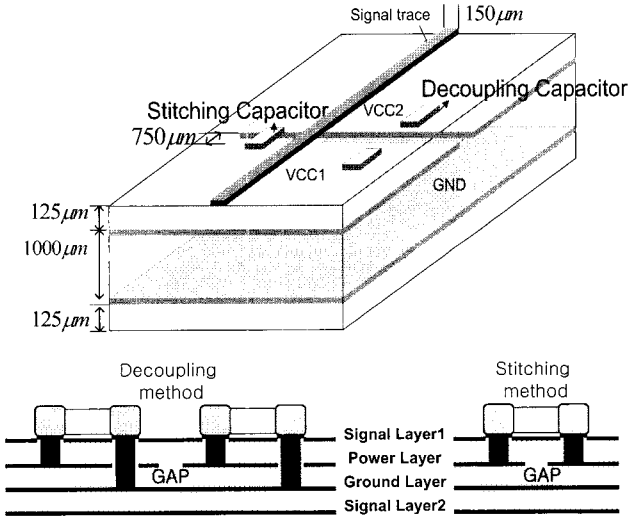

Fig. 1. PCB simulation structure with decoupling and stitching capacitor.

Manuscript received July 30, 2002 ; revised September 3, 2002.

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inductance effect. As shown in Fig. 2, the return current from driver at A cannot flow directly under the trace between *A-B*. Instead, it diverts around the ends of the power plane slot. The diverted current makes a large loop, increasing the inductance of signal path *A-B*, which effectively makes large loop antenna as a source of EM radiation. The stitching capacitor method provides direct return path on power plane, while the decoupling method creates return path below the slot by changing reference planes; this is, power plane to ground plane and vice versa. These current paths are depicted in Fig. 2.

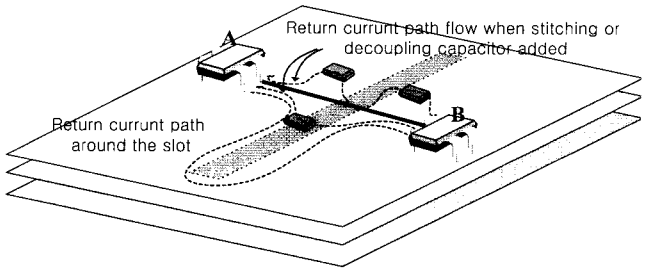

Fig. 2. Return current path in split power plane.

As a modeling effort, electrode resister and equivalent series inductance are included for capacitor model for better accuracy as seen in Fig. 3, and 3-D FDTD method generally used in the analysis of a planar structure is applied to analyze the modified circuit including lumped elements. The extended Maxwell equation including lumped element within one cell can be obtained by adding a component of a current source [5]~[7].

Extended Maxwell equation in FDTD

$$E_z^{n+1}(i,j,k)=E_z^n(i,j,k)+\frac{\Delta t}{\varepsilon_0}\nabla\times H^{n+1/2}(i,j,k)-\frac{\Delta t}{\varepsilon_0\Delta x\Delta y}I_L^{n+1/2}(i,j,k)$$

For modeling of capacitor C

$$E_z^{n+1}(i,j,k)=E_z^n(i,j,k)+\left(\frac{\frac{\Delta t}{\varepsilon_0}}{1+\frac{C\Delta z}{\varepsilon_0\Delta x\Delta y}}\right)\nabla\times H^{n+1/2}(i,j,k)$$

For modeling of resistance R

$$E_z^{n+1}(i,j,k)=\left(\frac{1-\frac{\Delta t\Delta z}{2R\varepsilon_0\Delta x\Delta y}}{1+\frac{\Delta t\Delta z}{2R\varepsilon_0\Delta x\Delta y}}\right)E_z^n(i,j,k)+\left(\frac{\frac{\Delta t}{\varepsilon_0}}{1+\frac{\Delta t\Delta z}{2R\varepsilon_0\Delta x\Delta y}}\right)\nabla\times H^{n+1/2}(i,j,k)$$

For modeling of inductance L

$$E_z^{n+1}(i,j,k)=E_z^n(i,j,k)+\frac{\Delta t}{\varepsilon_0}\nabla\times H^{n+1/2}(i,j,k)$$
$$-\frac{\Delta z(\Delta t)^2}{\varepsilon_0 L\Delta x\Delta y}\sum_{m=1}^{n}E_z^m(i,j,k)$$

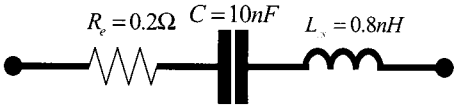

Fig. 3. Equivalent circuit model for 10 nF ceramic capacitor.

Ⅲ. Simulation and Result

The effect of the decoupling and stitching capacitors placed across the slot is simulated with 3D-FDTD. As depicted in Fig. 4, the absolute electric field strength is divided into four distinct pulses: forward and backward scattered pulses on the microstrip line and two excited pulses on the power plane slotline. These backward scattered pulse and slotline pulses bring about signal noise and EMI problems. When decoupling capacitors are placed between the power and ground planes, the return loss as well as insertion loss characteristics, especially in the low frequency region, are improved as shown in Fig. 5. This is mainly due to the return current path established by the capacitors. Even further improvement is possible with the use of stitching capacitors, which can be clearly seen in Fig. 5 and Fig. 6, due

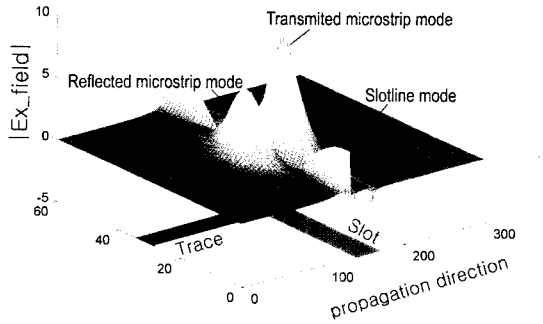

Fig. 4. Electric field intensity over the split power plane.

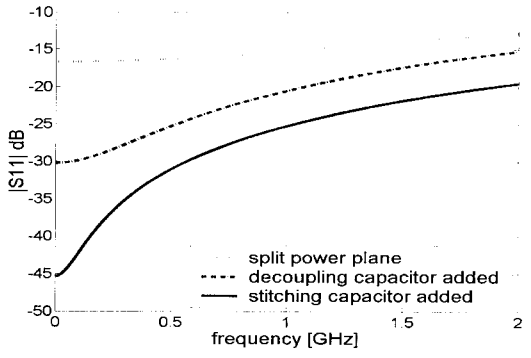

Fig. 5. Return loss of the split power plane.

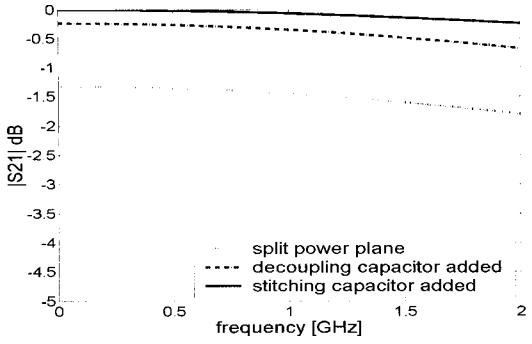

Fig. 6. Insertion loss of the split power plane.

to the reduced return current path compared to the previous approach.

The electromagnetic radiation caused by non-ideal return path is proportional to the total loss, and the calculation shows that the total loss $(1-|S_{11}|^2-|S_{21}|^2)$ can be reduced by adapting decoupling or stitching capacitor as shown in Fig. 7. Another point of signal integrity issue is the ground switching noise or ground bounce. Due to the slot in the reference plane, current is forced to flow along the slotline in the power plane and travel on ground plane, which causes ground bounce. The ground

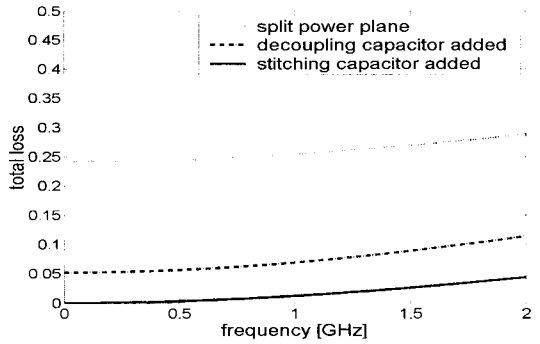

Fig. 7. Total loss of split power plane.

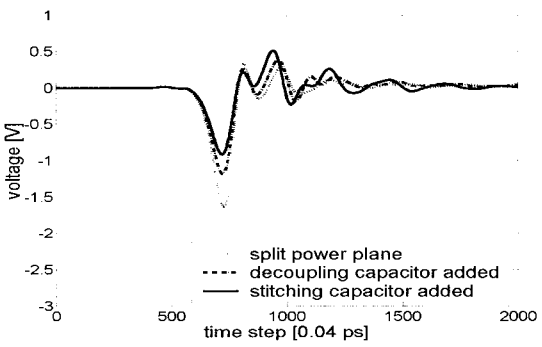

Fig. 8. Ground bounce of split power plane.

bounce also can be alleviated by stitching or decoupling capacitor as depicted in Fig. 7.

Ⅳ. Measurement

Measurement has been done in Pentium4® clock system made of FR-4 4-layer PCB. PCB is composed of a clock generator (ICS950201 Pentium4® clock generator) and multiple stitching /decoupling capacitors. Power layer is split into 3.3 V and 5 V as depicted in Fig. 9. In Fig. 10, the TDR measurement data shows that the impedance of trace crossing the split power plane increases from 60 Ω up to 66 Ω. This impedance change causes EM radiation and stitching capacitor could compensate for this impedance change.

Split power plane does not seriously distort digital signals, but may cause serious EM radiation. Fig. 11 shows that the stitching and decoupling capacitors around the split power plane have little effect on clock signal. However, EM radiation of the test vehicle measured in the chamber shows deep EMI problems as shown in Fig. 12 and Fig. 13, EM radiation has it's peak values at each harmonics of clock sources (33 MHz, 48 MHz, 66 MHz, 100 MHz). To reduce EM radiation, 10 nF stitching and decoupling capacitor are added around split power plane. In the

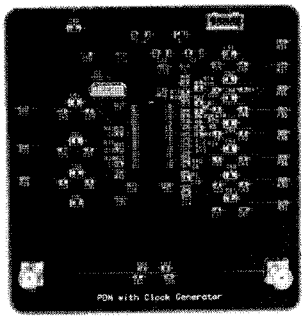

Fig. 9. Clock generator module in the multiple power distribution network.

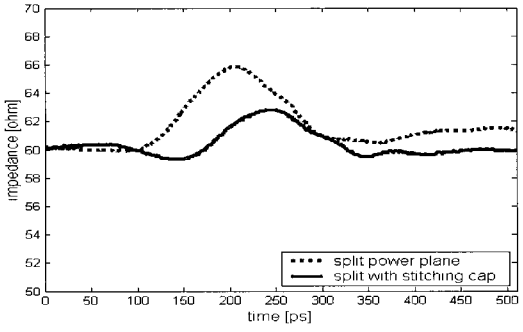

Fig. 10. TDR measurement data.

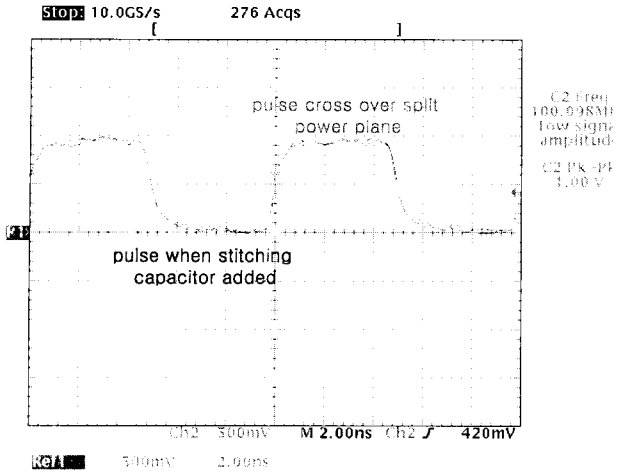

Fig. 11. 100 MHz signal measurement data.

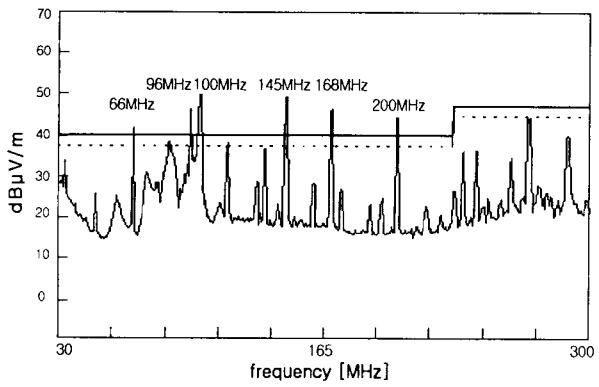

Fig. 12. EM radiation measurement in EMI chamber. (Low band: 30 MHz~300 MHz / split power plane)

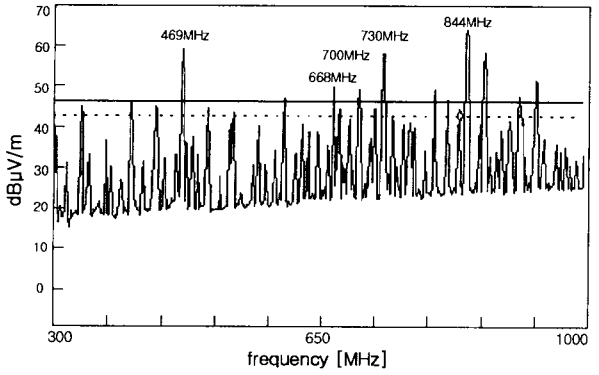

Fig. 13. EM radiation measurement in EMI chamber. (High band: 300 MHz~1 GHz / split power plane)

various measurements, if only stitching capacitor or decoupling capacitor is added, EM radiation is reduced by about 3 dB at each harmonics compared to the default split power plane PCB.

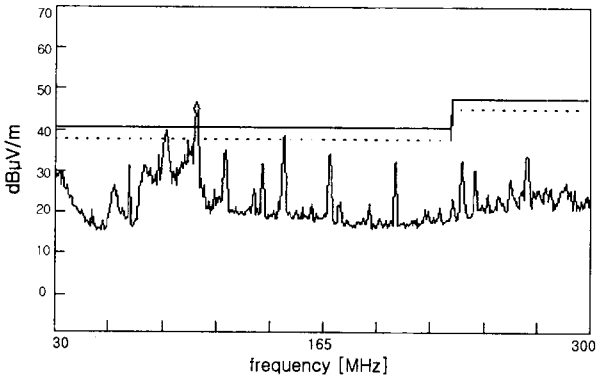

Fig. 14. EM radiation measurement in EMI chamber. (Low band: stitching / decoupling capacitors added)

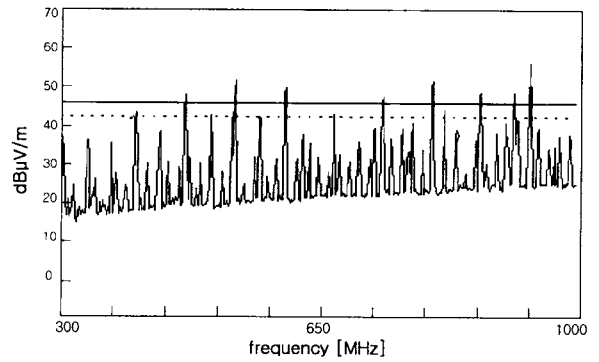

Fig. 15. EM radiation measurement in EMI chamber. (High band: stitching / decoupling capacitors added)

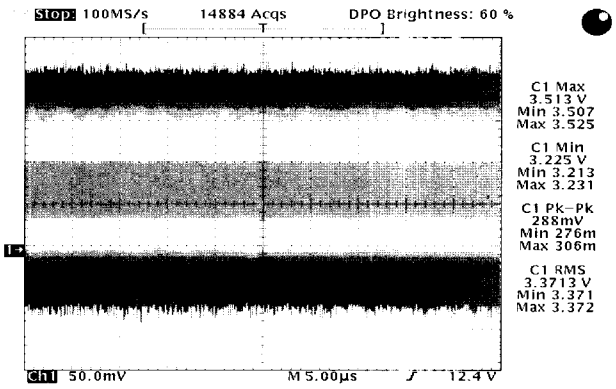

Fig. 16. Measured power plane noise.

However, if both stitching and decoupling capacitors are added, about 10 dB reduction at each harmonics is achieved as shown in Fig. 14 and Fig. 15. Therefore, effective design solution is to provide stitching capacitors with decoupling capacitors around the slot. Stitching and decoupling capacitors also reduce power plane noise. As shown in Fig. 16, 17 and Fig. 18, the power

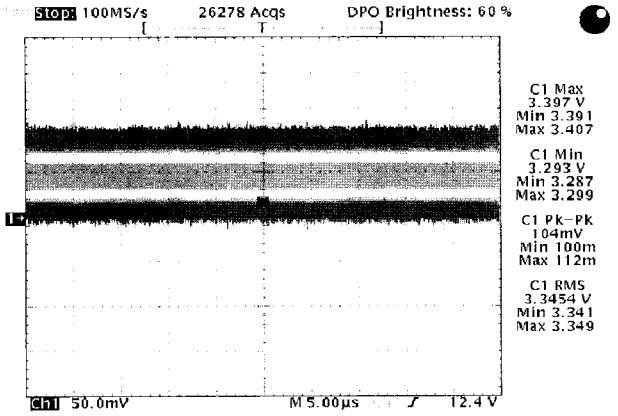

Fig. 17. Measured power plane noise. (stitching capacitor added)

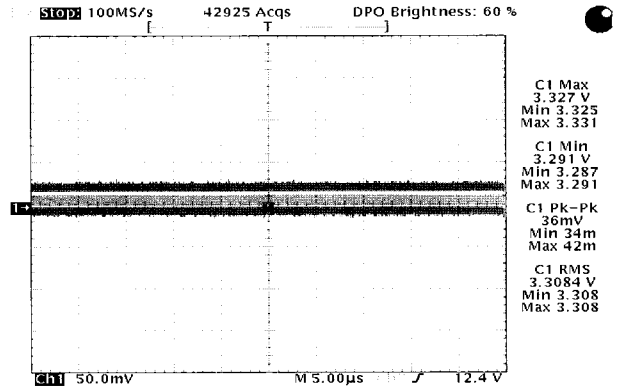

Fig. 18. Measured power plane noise. (stitching and decoupling capacitor added)

noise near the edge is 288 mV, which reduced to 36 mV after using decoupling and stitching capacitor around power plane discontinuity.

V. Conclusion

In this paper, signal integrity issues in the high-speed digital signal line passing through slot in the power plane are addressed based on 3D-FDTD simulations and various measurements. The effectiveness of the decoupling and stitching capacitors have been proven as far as the EMI problems concerns in practical PC main board design. With the stitching and decoupling capacitor around the split power plane, the return loss and total loss are effectively improved. Further, measurement result shows that EM radiation at each digital clock harmonics are reduced by about 10 dB.

The research was funded by the Ministry of Information and Communication, Republic of Korea, Project 02-06 "EMI/EMC problems in multilayered PCB".

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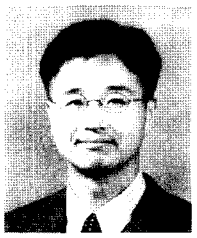

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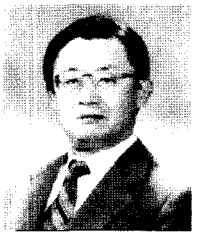

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