기 술 특 집

Poly-Si TFT Technology

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Abstract

Poly-Si TFT (Thin Film Transistor) technology are reviewed and discussed. Poly-Si TFTs fabricated on glass using low-temperature process were studied extensively for the application to LCD (Liquid Crystal Display) as well as to OLED (Organic Light Emitting Diode) Display. Currently, one of the application targets of the poly-Si TFT is emphasized on the highly functional SOG (System on Glass). Improvement of device characteristics such as an enhancement of carrier mobility has been studied intensively by enlarging the grain size. Reduction of the voltage and shrinkage of the device size are the trend of AM FPD (Active Matrix Flat Panel Display) as well as of Si LSI, which will arise a peculiar issue of uniformity for the device performance. Some approaches such as nucleation control of the grain seed or lateral grain growth have been tried, so far.

I. Introduction

Si TFT has been developed remarkably in the last 20 years and plays an important role for FPD application. The Poly-Si TFT had been developed for high-resolution LCD panel with peripheral circuit on quartz glass using high temperature process.[1] Subsequently, the poly-Si TFTs on low-cost glass were also applied to LCD panel with peripheral circuit, and have a further possibility for highly functional system i. e. SOG.[2] For the AM FPD panel, OLED Display of direct emission as well as LCD of indirect emission has been actively reported. The poly-Si TFT performance can be improved by optimizing the device structure and the effective crystallization process such as SPC (Solid Phase Crystallization),[3] ELC (Excimer Laser Crystallization) or MIC (Metal Induced Crystallization). Poly-Si TFT can be realized not only on glass but also on flexible metal or on plastic. Many efforts are being done on the optimization of the process and the improvement of the device characteristic. On the other hand, following a trend of lowering the voltage and shrinkage of device size by a requirement of display with high resolution as well as of conventional Si LSI, a uniformity issue including reliability for the TFT becomes important. In particular, pixel in AM FPD requires more uniform and stable characteristics of TFT than higher mobility for the driving. The characteristics of TFT, the improvement method and relating subject should be considered from a basic viewpoint of materials, process and/or device.[4]

II. Basic TFT characteristics and their improvement

Many efforts have been done to realize a high performance poly-Si TFT with high on-current and low off-current. In order to improve the TFTs as CMOS application, detailed study on carrier conduction should be done. In general, V_g-logI_d transfer curve for TFT can be divided into three regions under the biased condition, i. e., high on-current, a weak inversion and a leakage region. In each region, the characteristic depends strongly on the existence of trap states due to the defects in the Si film and at the SiO_2/Si interface.

1. Improvement of sub-threshold characteritic and reduction of leakage current

In order to get a sharp gate voltage swing, reducing the trap states density in Si film and at the interface of Si/SiO_2 is effective. As a result, threshold voltage can be controlled effectively in low voltage. In the weak inversion region, gate voltage swing(S) of TFT is given simply by,[5]

$$S = (kT/q)(1/\log_{10}e)(1 + qdN_T/C_{ox}) \quad (1)$$

N_T : Effective traps states density($cm^{-3}\ eV^{-1}$)

In order to obtain a sharp inverted characteristic in sub-threshold region, enlarging the oxide capacitance or decreasing the channel thickness as well as reducing the effective trap states density is important. As a result, controllability of V_{th} in low voltage is improved. In order to decrease the trap states density in the Si films or at the SiO_2/Si interface, improving the crystallinity in the Si channel, introduction of high quality with dense SiO_2 films and/or terminating the dangling bonds in the Si films by hydrogen passivation are considered. In the case of $N_T=0$, S gives an ideal value of 60mV/dec.(at R. T.), which corresponds to the S value for single-crystalline FD SOI(Fully Depleted Silicon on Insulator). Silicon oxide films deposited by high density plasma(HDP) sources of ECR(Electron Cyclotron Resonance) or ICP(Inductively Coupled Plasma) exhibit improved Si/SiO_2 interface and high breakdown voltage, due to low interface trap density, smooth interface and small number of carrier trapping site caused by the presence of less hydrogen.[6,7]

On the other hand, origin of leakage current is explained by a field emission from the trap in the depleted region near the drain,[8]

$$I_L \sim N_t \exp(V_g)\ V_d^m \quad (2)$$

N_t : Trap states density(cm^{-3})

Releasing the electric field near the drain is effective as well as reducing the trap states density caused by grain boundary for suppressing the leakage current. LDD(Lightly Doped Drain) or series connection of TFT is adopted. By adopting the structure, as hot-carrier immunity can be also improved, reliability evaluation of device is important.[9]

2. Enhancement of drain current for high performance characteristics

In general, carriers in poly-Si films are scattered not directly by lattice in the Si channel but by crystal defects such as the grain boundaries[10] or the fine defects which is distributed inside the grains. Therefore, conduction current in poly-Si TFT depends not only on the device geometry(L, W, t_{ox}) but also strongly on the carrier mobility. In order to increase a value of the field-effect mobility, high temperature thermal annealing and subsequent hydrogen passivation for the Si channel are necessary so as to decrease the defects density at the grain boundaries or in the grains and at the Si/SiO_2 interface.

For the poly-Si films with comparatively small grain size, existence of high trap states density suppresses the drain current. RTA(Rapid Thermal Annealing) at high temperature improves the device characteristics. Furthermore, single-shot ELA(Excimer Laser Annealing) improves the current drivability remarkably with keeping the grain size small.[11] As the localized defective regions in the films can be preferably melted by a shot of ELA, improvement in grain boundary or small defects is distinct.

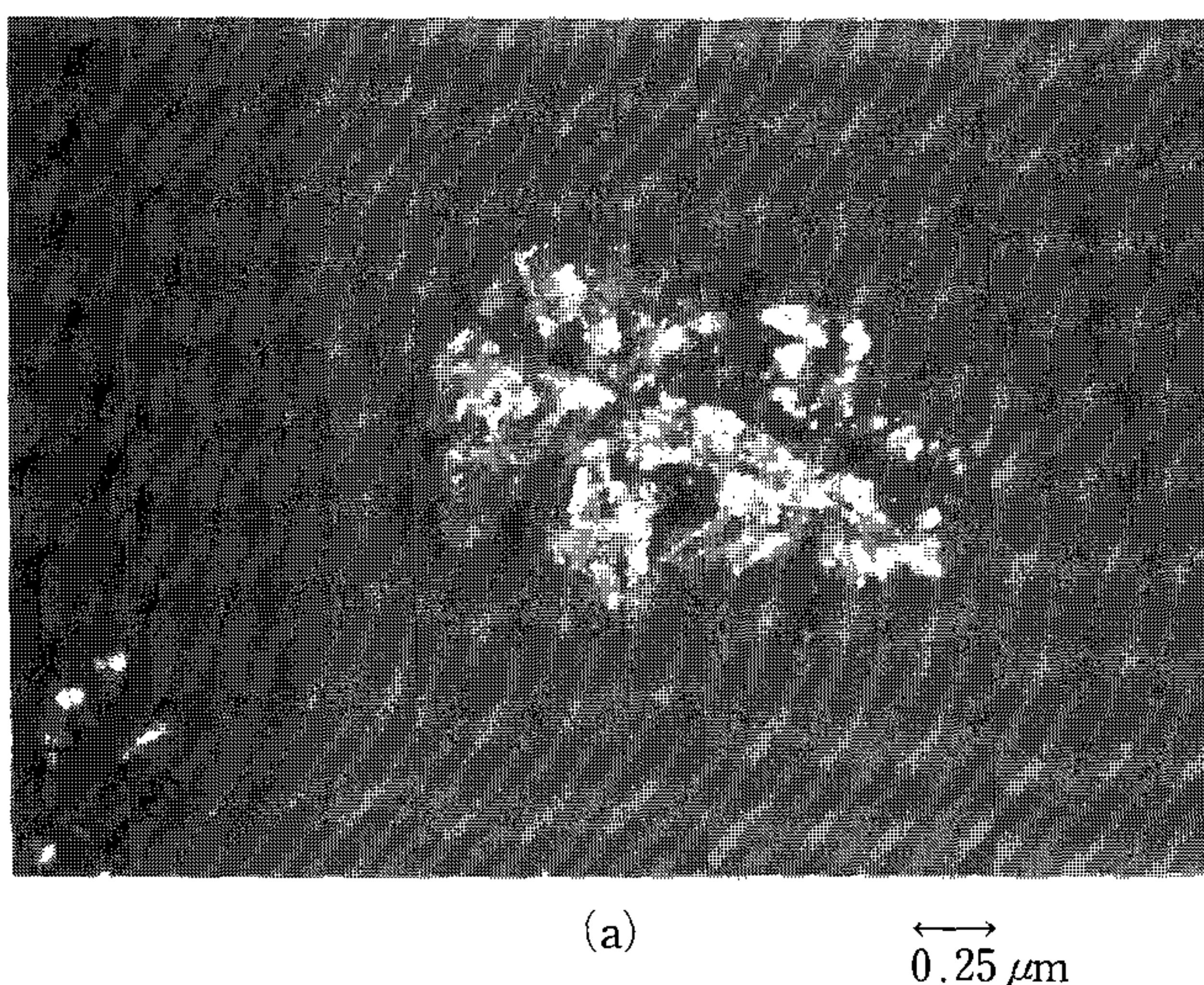
After long time of FA(Furnace Annealing) for amorphous Si films at around 600°C, large crystalline grains of dendrite shape($\gtrsim 1\mu m$) can be obtained.[3,5] ([Fig. 1]) After the SPC, electrical barrier height for electrons at the grain boundaries is very low[12] as well as the film obtained by ELA.([Fig. 2]) Although resultant drain current becomes high, there are still remained many small defects such as dislocation or twin boundaries. By performing a higher temperature FA or RTA or ELA subsequently after the SPC, the crystallinity improves, i. e. the trap states density due to the small in-grain defects decreases. In particular, ELA of controlled energy, which can melt mainly the defective region in the Si film instantaneously, improves drastically the crystallinity in the large grains and resultant TFT characteristic.[13,14]

On the other hand, to realize a lower temperature process, poly-SiGe channel using SPC has been proposed for TFT fabrication. By modifying the interface structure as $SiGe/Si/SiO_2$, getting higher current with sharp voltage swing is possible by suppressing the interface scattering.[15] Ni induced crystallization technique(MIC), which accelerates the lateral SPC speed, has also been studying intensively as a lower temperature process.[16,17] By incorporating Ni

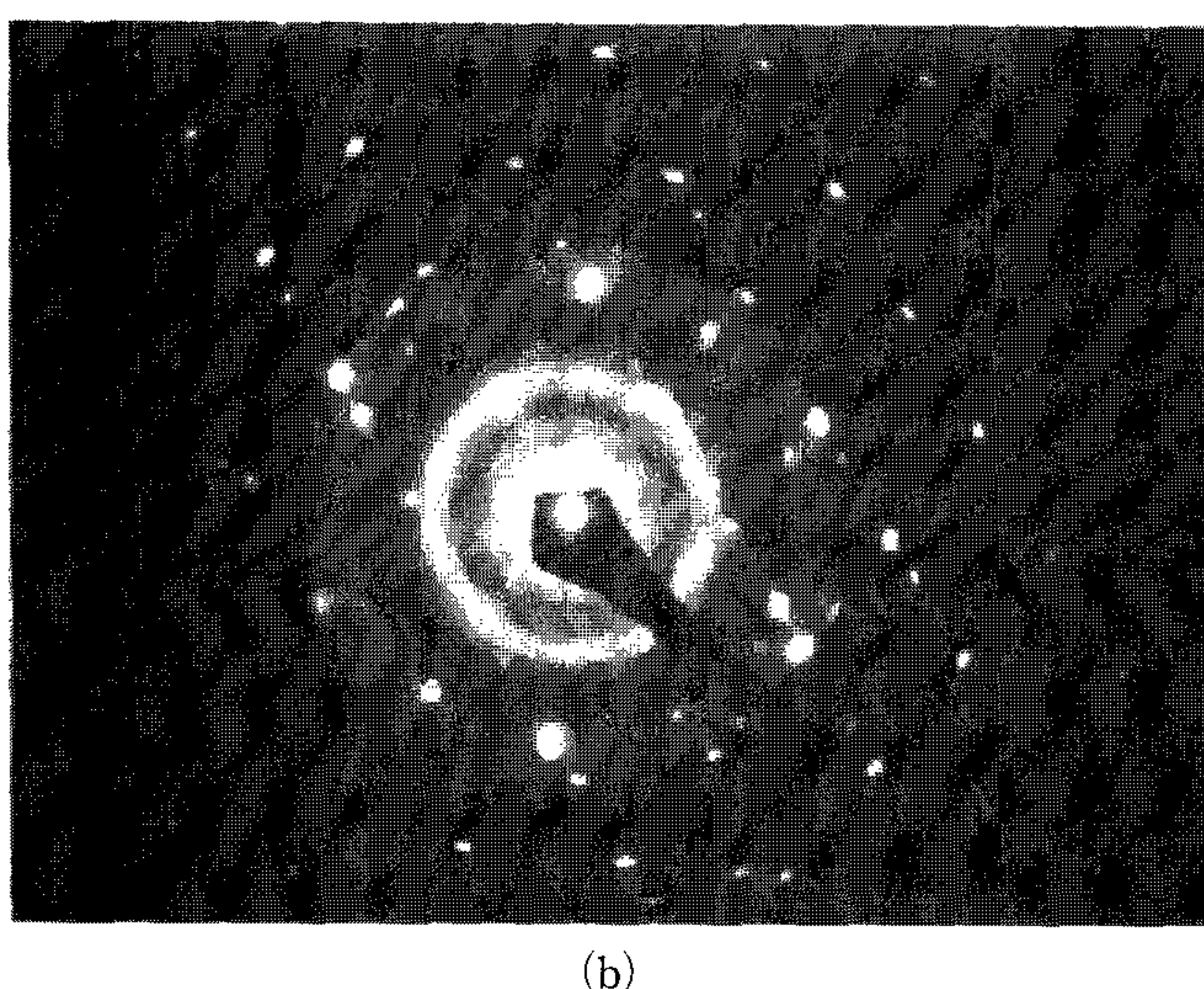
into the Si films, a few microns of needle-like long grains can be obtained.

Excimer laser with UV (Ultra-Violet) pulsed beam can heat up only Si surface or thin Si layer without giving a heating damage under substrate. Direct ELC on amorphous Si has been studied intensively. In order to get a larger grain size, ELC with heating of substrate is effective, so as to control its solidification velocity.[18, 19] Also, notable lateral grain growth by optimizing the energy condition with multi-shots ELC or ELA has been reported.[20, 21, 22, 23] (Fig. 3, 4) Lateral crystallization effect under thermal slope is more drastical.[23, 24] As the ELC of sufficient energy density can melt the Si films, the grain boundary barrier height for the laser annealed films is low as well as for the films after SPC, and the crystallinity in the grains for the film of ELC is better than that for the case of only SPC although the surface flatness should be inferior.

In order to produce the maximum performance of TFT characteristics, optimum process are required for the thin source and drain and for the gate electrodes of low resistivity and of the ohmic contact. Efficient activation, another doping and/or silicidation compatible with low temperature process have been studied.[25, 26, 27]

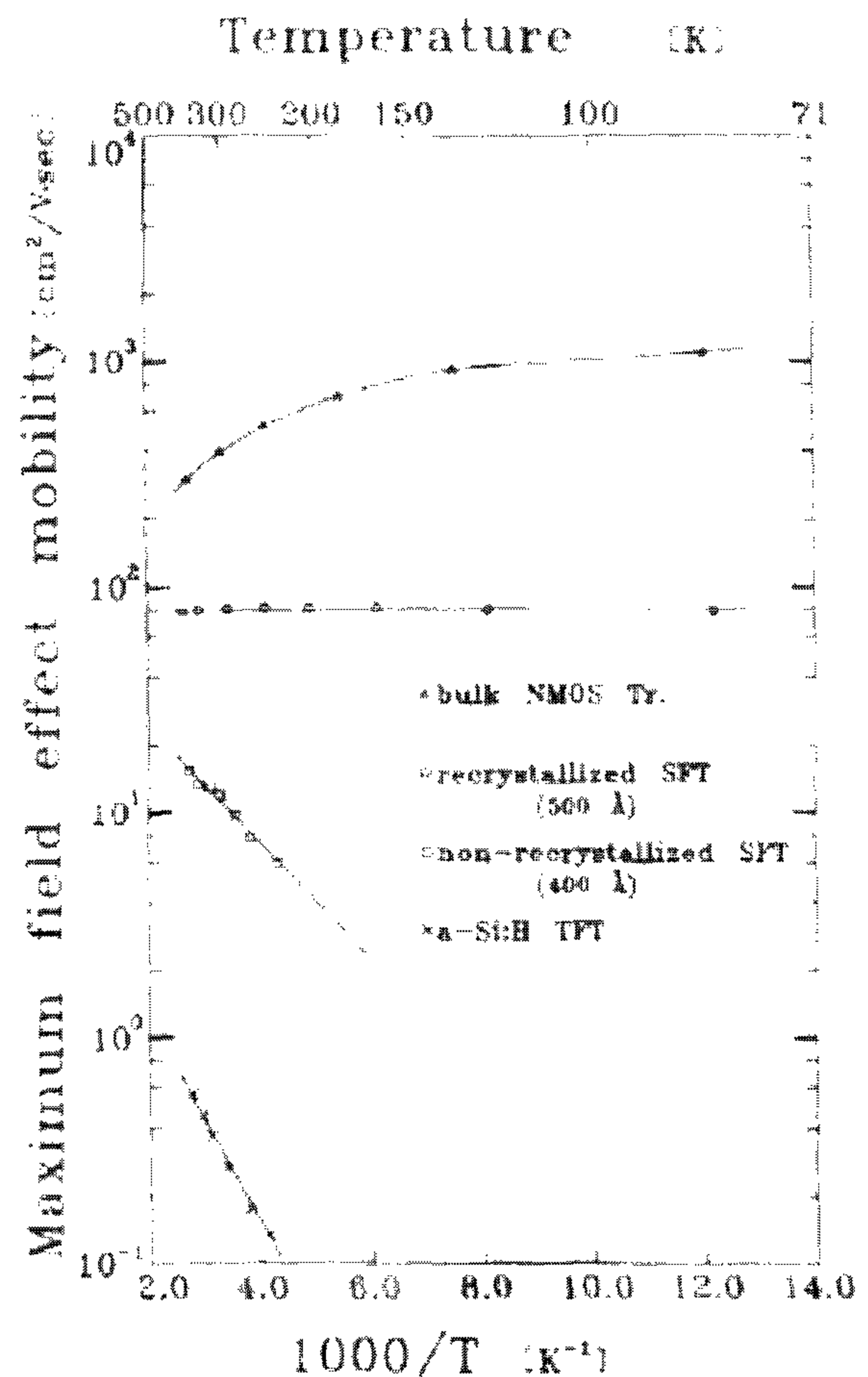


(a) 0.25 μm

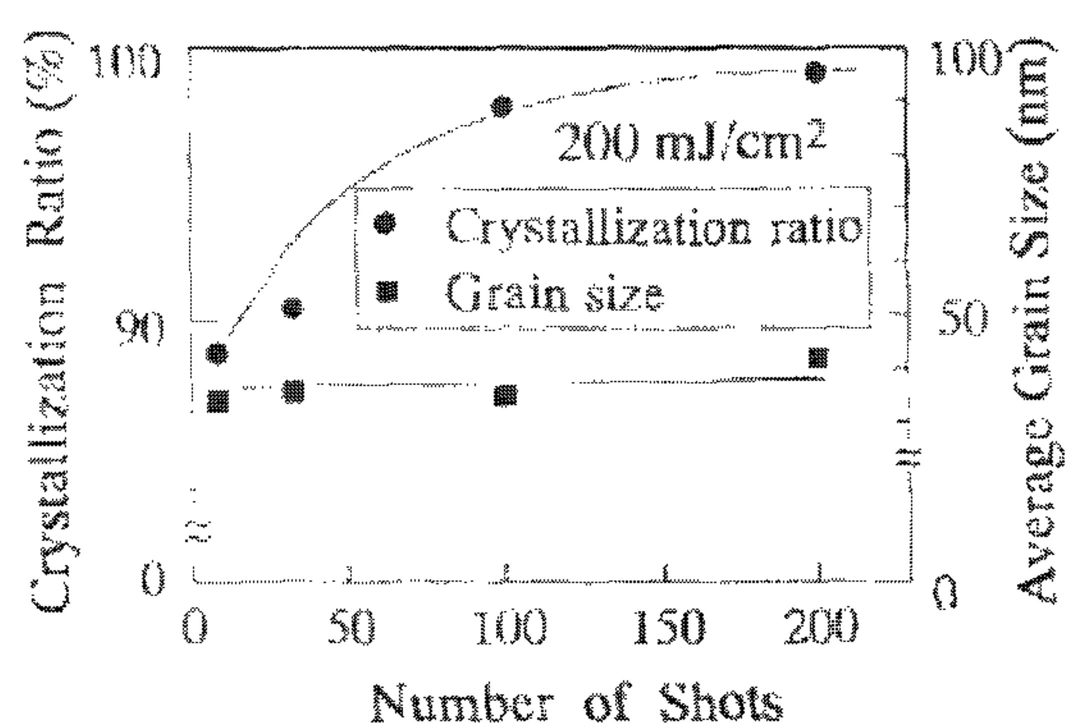


(b)

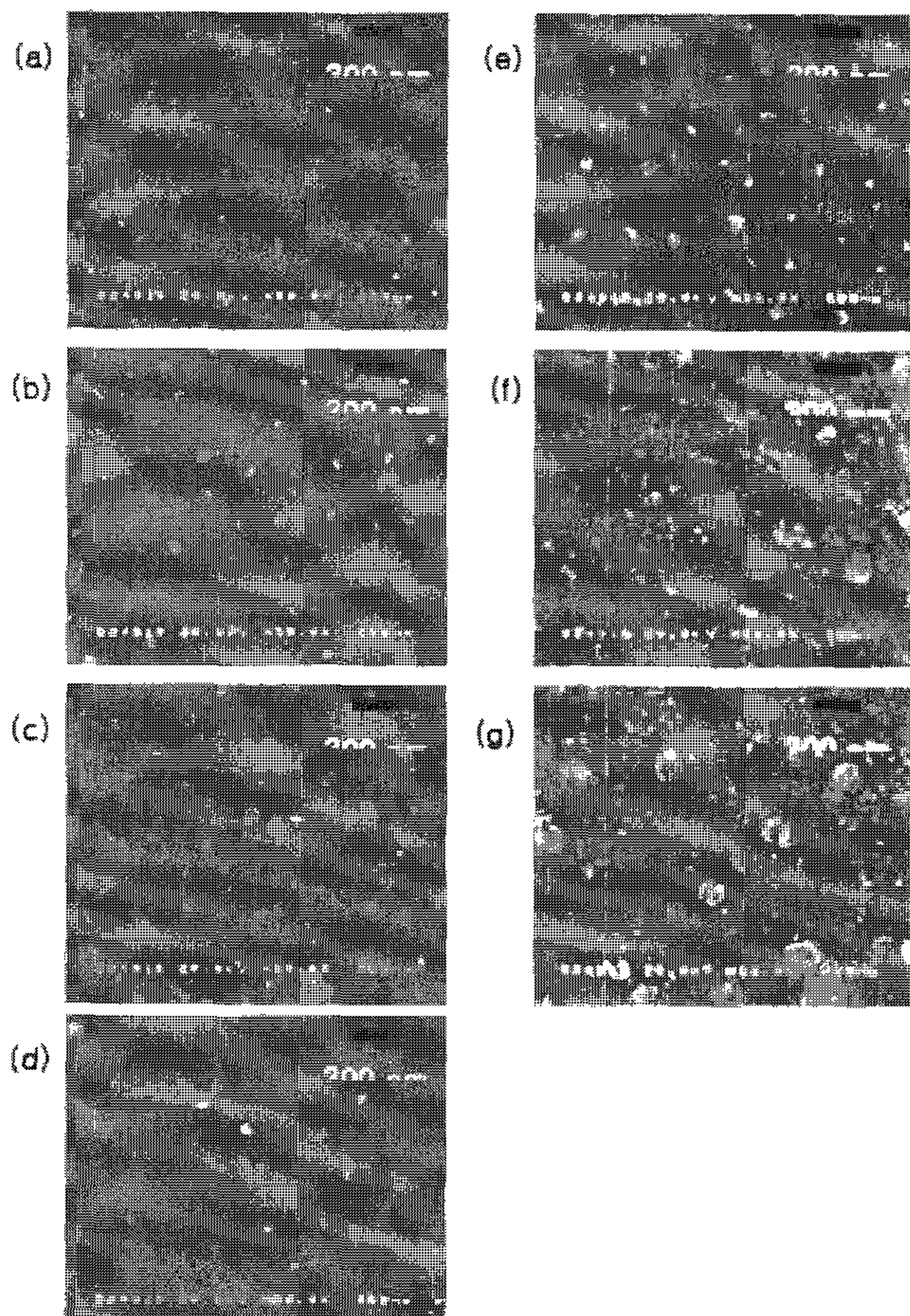
[Fig. 1] TEM image of one typical grain from amorphous phase (SPC).[5]



[Fig. 2] Temperature dependence of maximum field-effect mobility for various Si MOS FETs.[12]



[Fig. 3] Relationships between the crystallization ration, the grain size and the number of shots.[21]



[**Fig. 4**] SEM images as a function of multi-shots. (ELC).[22]

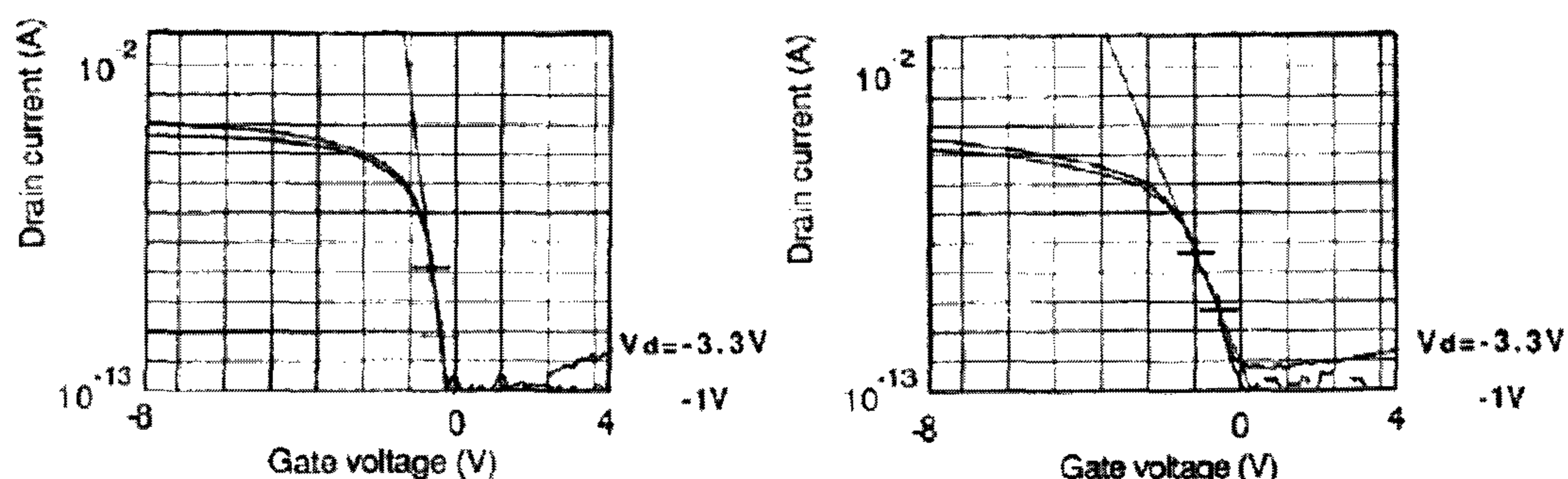
Ⅲ. The subject for a reduction of driving voltage

Poly-Si TFTs have been practically applied to high density SRAM (Static Random Access Memory) in LSI[28] previously, and for AM FPD today. Some results for the short channel TFT have been reported.[29] Today, not only an improvement but also uniform device characteristics are required for poly-Si TFTs following a trend as a reduction of driving voltage and a shrinkage of pixel size in FPD as well as in Si LSI. The smaller the size or the lower the driving voltage, the device characteristics depend more sensitively on the crystallinity. In principle, the larger the grain size, the higher the TFT performance, the more degrades the uniformity.[30] In pixels, the mobility value of TFTs is not required so high as in peripheral circuits for AM LCD or even for AM OLED display panel. a-Si TFTs of low mobility still have a higher advantage in terms of uniformity for the LCD of large panel.[31] Also, for OLED addressing, the TFTs and their process having optimum grain size should be developed so as to suit the optimum circuit design.[32]

In order to realize uniform and high performance TFTs, fabricating one TFT in each single-crystal grain, i. e. location controlled crystallization method, has been proposed.[33, 34] Excellent SOI-like characteristics have been reported by fabricating a small size TFT in a single-crystal-like grain.[30, 35, 36] ([Fig. 5]) Results of almost single crystal-like TFT characteristic have been reported by adopting a lateral grain growth techniques such as longer pulsed beam or CW laser.[37, 38] In order to ensure the highly uniform and higher performance TFT characteristics, basic research on the device and process, which improves the gate oxide, the interface and the crystalline Si films taking into consideration of orientation control must be further studied.[39]

Ⅳ. State of the art of Si TFT on panel

Currently, poly-Si TFT is studied for the application of driving circuit for LCD or OLED. Today, for the FPD, more functional and/or unique application by mounting the high performance TFTs on panel is wanted. In general, glass is already popular as an under substrate. By using the short channel TFTs with high performance and uniform characteristic, functional logic circuits or even the MPU level should be possible



[**Fig. 5**] Typical TFT characteristic for a single-crystal-like grain (a) and for poly-Si grains (b).[30]

to mount. On the other hand, a plastic display panel, which is light and has a strong robustness, is wanted. As this material, such as PES(PolyEtherSulphone), PET(PolyEthyleneTerephthalate) or PI(PolyImide) has a poor thermal hardness and large thermal expansion property, further lower temperature process is required for the TFT fabrication. Related studies have been reported.[40, 41] Recently, unique transfer process techniques from one temporal substrate to another plastic are proposed as a fabrication method.[42, 43] On the other hand, even on the metal[44], poly-Si TFT can be fabricated as for a reflective type LCD or OLED display. A stable flexible material with small thermal expansion for the substrate and a modified film structure against thermal and chemical damage are required.

As for a monitor for digital camera or a cellular-phone, flexible substrate using low temperature poly-Si TFT process with high robustness has a higher advantage. Mounting the functional circuits such as a peripheral circuit, DAC(D/A Converter), memory and even MPU(Micro Processor Unit) is expected.[2] The poly-Si TFT will contribute as an informational terminal between display and telecommunication system.

V. Summary

An improvement of device performance and a relating subject including the possibility were briefly reviewed and were described for the TFT with on glass or on panel. High performance TFT having uniform characteristics are expected. Currently, for an active matrix display, high functionality is expected by mounting additional circuits such as a memory, a DAC etc. including MPU. Higher image quality with lower voltage driving is expected using addressing OLED although the requirement of uniformity for the fine patterned TFT characteristic becomes more severe. By overcoming the technical subject lying ahead, coming SOG era using TFT should be possible.

VI. Acknowledgement

Authors would like to acknowledge to the scientists in SAIT and professors in Sungkyunkwan University for encouragement. Authors also acknowledge to previous co-researchers, and to the scientists in this field.

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