An Ultra Wideband Low Noise Amplifier in 0.18 μm RF CMOS Technology

Ji-Hak Jung · Tae-Yeoul Yun · Jae-Hoon Choi

Abstract

This paper presents a broadband two-stage low noise amplifier(LNA) operating from 3 to 10 GHz, designed with 0.18 μm RF CMOS technology. The cascode feedback topology and broadband matching technique are used to achieve broadband performance and input/output matching characteristics. The proposed UWB LNA results in the low noise figure(NF) of 3.4 dB, input/output return loss(S_{11}/S_{22}) of lower than -10 dB, and power gain of 14.5 dB with gain flatness of ± 1 dB within the required bandwidth. The input-referred third-order intercept point(IIP_3) and the input-referred 1-dB compression point(P_{1dB}) are -7 dBm and -17 dBm, respectively.

Key words : CMOS, Cascode, Feedback, Low Noise Amplifier, Ultra Wideband.

Ⅰ. Introduction

Recently, considerable interest in ultra wideband (UWB) technology centers on its potential applicability for short range, high-speed wireless communications. In general, this technology has several advantages such as a low complexity, low cost, low power consumption, and high data rate wireless connectivity among devices within or entering the personal operating space. UWB communications are allowed at a very low average transmit power compared to more conventional(narrow-band) systems that effectively restricts UWB to short range. UWB is, thus, a candidate of physical layer mechanism for IEEE 802.15 Wireless Personal Area Network(PAN) for short range and high rate connectivity that complements other wireless technologies.

The LNA is one of the most important building blocks in front end of a telecommunication system. LNA's purpose is to amplify the received signal from the antenna with as little distortion and additional noise as possible. Its performance determines the overall system sensitivity. This can be achieved by designing an appropriate matching network placed between the antenna and the amplifier. However, the design of an LNA is full of trade-offs between gain, noise figure, input matching linearity, and power consumption.

In this paper, a new LNA is proposed with a cascode feedback topology and impedance matching techniques, which meets requirements of the multi-band orthogonal frequency division multiplexing(OFDM) for UWB systems in the noise and bandwidth simultaneously.

Ⅱ. Requirement of UWB LNA

Recently, many proposals have been made to regard the UWB PHY layer for IEEE 802.15.3a. One of the promising proposals for multi-band UWB system is based on frequency-hopped QPSK OFDM modulation.

As we know, the first stage of the receiver is commonly the LNA whose main function is to provide enough gain to overcome the noise of subsequent stages such as mixer, filters, but not so much to cause the mixer overload. Secondly, the LNA should add as little noise as possible to minimize the impact on the overall noise performance. For wireless applications, the LNA noise figure(NF) should be maintained below 2~3 dB because unavoidable losses of RF filter remain little noise budget for other active blocks. According to the proposed OFDM for IEEE 802.15.3a, the noise figure (NF) for the RF front-end requires 8.6 dB approximately[1]. This results in that the LNA's NF should be less than 4 dB[2],[3]. Therefore, when the LNA's gain and NF are chosen as 12 dB and less than 4 dB, respectively, the receiver sensitivity requirement for UWB application[1] can be satisfied. Moreover, to avoid reflections from the transmission line connecting the off-chip antenna to on-chip LNA, an LNA must also present 50 Ω to the input source.

Ⅲ. Circuit Design

As shown in Fig. 1, the proposed CMOS LNA is composed of two stages, designed with Agilent's

Manuscript received March 23, 2005 ; revised July 25, 2005. (ID No. 20050323-007J)
Department of Electronics and Computer Engineering, Hanyang University, Seoul, Korea.

Advanced Design system(ADS) and Samsung's 0.18 μm RF CMOS technology based on the standard BSIM3v3 model. The first and second stages are designed to resonate at 4 and 8 GHz with R_o, C_t, and L_t, respectively. This stagger tuning technique is used to yield a flatter and broader bandwidth. The first stage consists of cascoded MOSFETs, shunt feedbacks, and input matching networks.

The merit of this cascode topology is its negligible Miller effect on the transistor M_1. Secondly, transistor M_2 has a high output impedance at its drain to improve the reverse isolation[4], thus increasing the stability of the LNA.

One of the most critical steps in the LNA design procedure is the noise optimization[3]. For any arbitrary bias and frequency conditions, the source impedance Z_s is selected to minimize the noise figure. The optimum L_s in shown Fig. 1 also controls the noise performance of the proposed architecture. In general, noise factor F can be expressed as follows,

$$F = F_{\min} + \frac{R_n |Y_s - Y_{opt}|}{G_s} \tag{1}$$

where F_{min} is the minimum noise factor, R_n the noise resistance, Y_s the source admittance($Y_s = 1/Z_s$), Y_{opt} the optimum source admittance($Y_{opt} = 1/Z_{opt}$), and G_s the real part of the source admittance. From Eq. (1), Noise optimization should be achieved by the condition of $Z_s \approx Z_{opt}$.

In this study, the simultaneous noise and input matching technique represented in [5] is adopted. The input impedance Z_{in} in Fig. 1, assuming that the feedback effect is negligible, can be expressed as

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{2}$$

where L_s is the source degeneration inductance, g_m is the transconductance, and C_{gs} the gate-source capacitance. As can be seen from Eq. (2), the source degeneration generates the real part at the input impedance. This is important because there is no real part in Z_{in} without L_s. The condition that allows the simultaneous noise and input matching is

$$Z_{opt} = Z_{in}^* \tag{3}$$

The design parameters that can satisfy Eq. (3) are V_{gate}, the transistor width(or C_{gs}), and L_s[5]. The first stage's transistor size and bias point should be optimized for the low NF because both factors seriously affect the noise performance and also the first stage dominantly contributes to the total NF. The detail procedure that the width of the transistor M_1 and bias point are chosen would be described in [5].

However, the simultaneous noise and input matching technique is not suitable for wideband applications. In the proposed LNA, The large values of feedback resistors R_f(900~1,100 Ω) are employed to produce the wideband input impedance matching, without affecting the noise figure significantly. The resistive and capacitive shunt feedbacks(R_f, C_f) also improve the better stability, gain flatness, and bandwidth[6]. In addition, the input matching network consists of a source degeneration inductance L_s and a gate inductance L_g[7]. L_s is achieved with a transmission line due to low inductance value, hence avoiding the use of additional area for an on-chip spiral inductor.

Finally, the gate optimum widths of M_1 and M_2 and the gate bias voltage(V_{gate1}) for the first stage are designed at 160 μm and 0.8 V, respectively.

The second stage should consider the linearity performance because the last stage is a prominent contributor to degrade the linearity[2]. For a cascaded amplifier, the total input-referred third-order intercept point($IIP_{3,\,total}$) is expressed as

$$\frac{1}{IIP_{3,\,total}} \approx \frac{1}{IIP_{3,1}} + \frac{\alpha_1^2}{IIP_{3,2}} + \frac{\alpha_1^2 \beta_1^2}{IIP_{3,3}} + \cdots \tag{4}$$

where α_1 and β_1 are the linear gains for the first and second stages, respectively. Eq. (4) shows that the last stage's IIP_3 significantly affects the total IIP_3. Thus, the proper device size and bias condition of the second stage are designed for the high gain and linearity improvement with restricted power consumption. The gate width of 80 μm and 160 μm are chosen for M_3 and M_4, respectively. The gate bias voltage(V_{gate2}) of 0.85 V is chosen for M_3.

Tank circuits of L_t and C_t are also designed to resonate at 4 and 8 GHz for each stage, which yield a flatter and broader bandwidth. R_o and C_t bypass networks with the L_tC_t tank are integrated with dc bias lines to ensure the gain and stability at a low frequency.

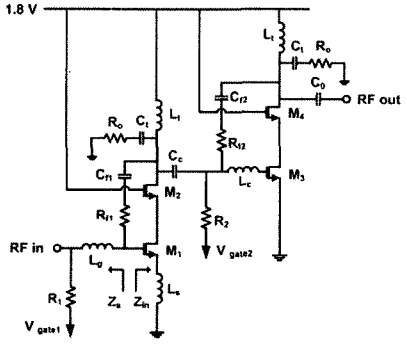

Fig. 1. Proposed two-stage UWB LNA with the cascode and feedback.

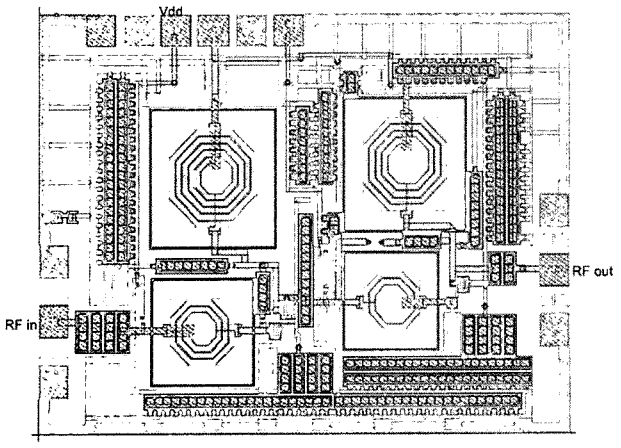

Fig. 2. Layout of the designed UWB LNA(size=0.8 × 1.1 mm^2).

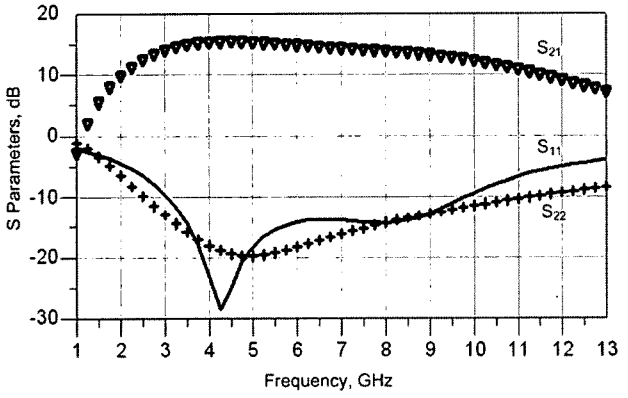

Fig. 3. Input/output return losses(S_{11}/S_{22}) and gain(S_{21}).

It also affects the broadband output matching. A coupling capacitor $C_{coupling}$ is used to couple the RF signal from M_2 to M_3. L_c can improve the gain and NF of the amplifier at a high frequency. A large resistance of R_1 and R_2 is chosen to reduce the noise contribution from the bias circuits and the loading effect on the signal path.

Ⅳ. Post-Layout Simulation Results

The post-layout circuit simulation is carried out using a Cadence SpectreRF including the parasitic effects of the actual devices. When 1.8 Volts is supplied, a total dc-current consumption of the proposed LNA is only 18 mA. Due to a high sheet resistance of the poly gate of RF MOSFET, a multi-finger layout technology is adopted to reduce the noise of the RF MOSFET's gate resistance and to improve its RF performance. The final layout is shown in Fig. 2. The chip size is mainly determined by the size of on-chip inductors. The total

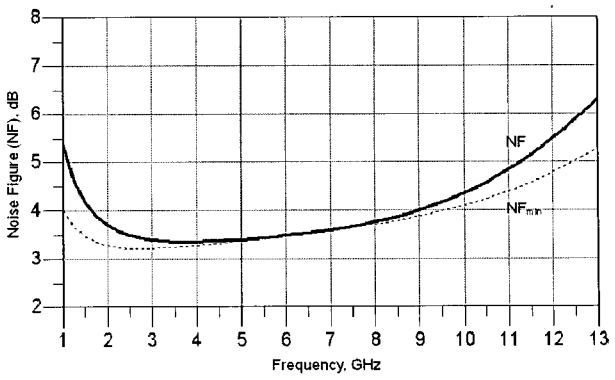

Fig. 4. Noise figure(NF).

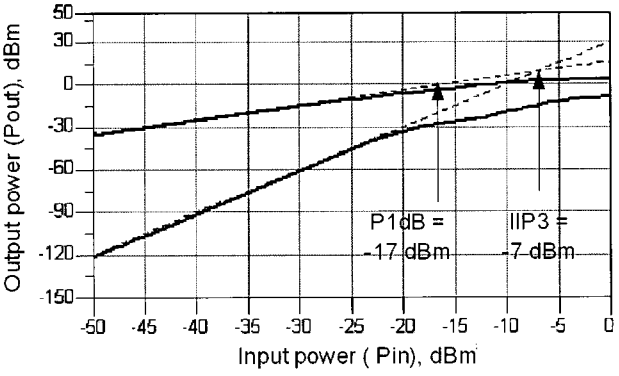

Fig. 5. Input-referred third-order intercept point(IIP_3) and 1-dB compression point(P_{1dB}).

chip area has 0.8 × 1.1 mm^2 including pads. Input/output return losses(S_{11} and S_{22}) of less than −10 dB are obtained over 3 to 10 GHz, as shown in Fig. 3. This proves the effectiveness of the broadband matching realized by the matching networks, shunt feedback, and LC tanks. In addition, the designed LNA achieves the maximum gain(S_{21}) of 15.5 dB with flatness of 2 dB over the whole frequency band. The noise figure is illustrated in Fig. 4 and has 4.3 dB in the worst. The low value NF is attributed to the optimum transistor size and bias point at the first stage. To observe the non-linear behavior, two-tone signals with equal power levels at several frequencies are applied to LNA. Both tones are swept from −50 to 0 dBm. Fig. 5 indicates that the LNA has the input-referred third-order intercept point(IIP_3) of −7 dBm and the input-referred 1-dB compression point(P_{1dB}) of −17 dBm at 4.5 and 4.51 GHz. Fig. 6 shows IIP_3 versus frequency for the proposed LNA. IIP_3 is higher than −8.5 dBm in the 3 to 9 GHz range. The post-layout circuit simulation results are summarized in Table 1. These results demonstrate that the proposed UWB LNA achieves the very good linearity even with the low noise figure.

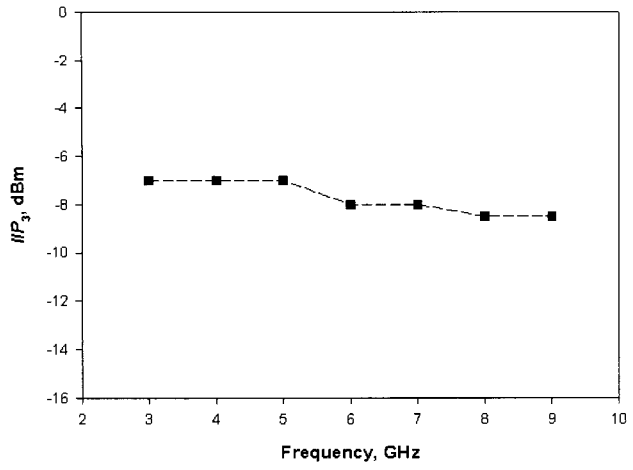

Fig. 6. IIP_3 versus frequency.

Table 1. Summary of post-layout simulation results.

Parameters	Post-layout circuit simulation
Frequency range	3~10 GHz
S_{21}	15.5~13.5 dB
S_{11}, S_{22}	< −10 dB
NF	3.4~4.3 dB
P_{1dB}	−17 dBm at 4.5 GHz
IIP_3	−7 dBm at 4.5 GHz
Power consumption	32.4 mW(V_{dd}=1.8 V, 18 mA)

V. Conclusion

In this paper, an ultra wideband(UWB) LNA with cascode feedback and impedance matching techniques has been presented. The circuit consists of two stages, whereby design issues of noise and linearity were almost separated into each stage; the first stage contributed to optimise the best noise performance and the second stage to improve the LNA's linearity. The proposed LNA could be readily implemented for UWB systems.

This research was supported by University IT Research Center Project(INHA UWB-ITRC), Korea.

References

[1] "Multi-band OFDM physical layer proposal for IEEE 802.15 Task group3a", *IEEE P802.*, 15-03/268r2, Nov. 2003.

[2] B. Razavi, *RF Microelectronics*, Prentice-Hall, 1998.

[3] G. Gonzalez, *Microwave Transistor Amplifiers*, Prentice-Hall, 1984.

[4] D. Shaeffer, T. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier", *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, 1997.

[5] T. K. Nguyen, C. H. Kim, G. J. Ihm, M. S. Yang, and S. G. Lee, "CMOS low-noise amplifier design optimization techniques", *IEEE Trans. Microwave Theory and Techniques*, vol. 52, no. 5, pp. 1433-1442, 2004.

[6] F. Ali, C. Hutchinson, and A. podell, "A novel cascode feedback GaAs MMIC LNA with transformer-coupled output using multiple fabrication process", *IEEE Microwave and Guided Wave Letters*, vol. 2, no. 2, pp. 70-72, 1992.

[7] K. Yu, Y. Lu, D. Huang, D. Chang, V. Liang, and M. Chang, "24 GHz low-noise amplifier in 0.18 CMOS technology", *IEE Electron. Lett.*, vol. 39, no. 22, pp. 1599-1560, 2003.

Ji-Hak Jung

He received the B.S. degree from Cheongju University and the M.S. degree from Dongguk University Korea in 1999 and 2002, respectively. Since 2002 he is currently working toward the Ph.D. degree at Hanyang University, Korea. His current research interests are RF IC, antennas design, and RF transceiver.

Tae-Yeoul Yun

He received the B.S. degree from Kyungpook National University, the M.S. degree from KAIST(Korea Advanced Institute of Science and Technology), Korea, and the Ph.D. degree from Texas A&M University, Texas in 1987, 1989, and 2001, respectively. From 1989 to 1996, he worked for the optical telecommunication system group, ETRI. From 2001 to 2003, he was with Triquint, Dallas, Texas. Since 2003 he has been an assistant professor of dept. of electronics and computer engineering, Hanyang University, Korea. His research interests are passive and active microwave circuits, antenna systems, and high speed optical telecommunication devices and systems.

Jae-Hoon Choi

He received the B.S. degree from Hanyang University, Korea, the M.S. degree and the Ph.D. degree from Ohio State University, Ohio in 1980, 1986, and 1989, respectively. From 1989 to 1991, he was a research analyst with Telecommunications Research Center at Arizona State University, Tempe, Arizona. He had been with the Korea Telecom as a team leader of Satellite Communication Division from 1991 to 1995. Since 1995 he has been a professor of dept. of electronics and computer engineering, Hanyang University, Korea. His research interests are antenna, microwave circuits design, and EMC.