SIPAC

No.	IP Name (Type / Format)	Seller	Category	Description
1	ST NAND128-A FLASH MEMORY VITAL MODEL (VITAL model / VHDL)	HDL Design House (http://www.hdl-dh.com)	Memory Element 〉Flash Memory	ST's NAND Flash 528 Byte/264 Word Page family is available in densities of 128Mbit to 1Gbit with supply voltages of 3V or 1.8V to suit the main applications.
2	ADSSCG – All-Digital Spread Spectrum Clock Generator (SSCG) (Hard IP / VHDL, Verilog, GDS II, Spice)	DFM Ltd. (http://www.dfm4vlsi.com)	Analog & Mixed Signal 〉PLL/DLL	The ADSSCG is a logic core that spreads the frequency of the input reference clock. Activating this core reduces the EMI (Electro-Magnetic Interference) caused by the clock significantly. It is a simple and low-cost alternative to the commonly-used ferrite-beads.
3	GPDLL – General Purpose all-digital DLL core (Hard IP / VHDL, Verilog, GDS II, Spice)	DFM Ltd. (http://www.dfm4vlsi.com)	Analog & Mixed Signal 〉PLL/DLL	The GPDLL is a logic core that provides most of the clocking and timing management features that are required in many VLSI systems. It can be used for clock de-skewing, clock frequency multiplication, splitting the period to phases, controlling slave delay lines and correcting the duty cycle.
4	HPDLL – High performance all-digital DLL core	DFM Ltd. (http://www.dfm4vlsi.com)	Analog & Mixed Signal 〉PLL/DLL	The HPDLL is a logic core that provides the key clocking and timing management features that are required for high speed VLSI systems. It can be used for clock de-skewing, frequency doubling, controlling slave delay lines and duty cycle correction.
5	Soft Decision Viterbi Decoder for wLAN (Soft IP / VHDL)	Hoseo University (http://www.hoseo.ac.kr)	Data Transmission 〉Error Correction/Detection 〉Viterbi	– The DATA field made up of Service, PSDU, tail and pad parts – It is 1/2, 2/3, 3/4 that coding rate in convolutional code(k=7) – polinomial equation of convolution encoder is 133(8), 171(8) in rate=1/2
6	MAC-PHY Layer Interface Controller for WLAN (Soft IP / VHDL)	Hoseo University (http://www.hoseo.ac.kr)	Wireless Communications 〉802.11	– This function simplifies the PHY service interface to the IEEE 802.11 MAC service. – PLCP preambles, SIGNAL(One OFDM Symbol), DATA(Variable Number of OFDM Symbols)
7	Pipelined SEED Processor on FPGA (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	There is a limit for already established proposal method to improve speed, because it performs F function in a form of pipe system, which is same as iterative method. Therefore, SEED cryptograph processor is improved in consideration of pipeline structure.
8	Pipelined AES (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	Round block of AES is processed in parallel, and the engine is materialized, which is suitable for specific application by each round block using pipeline technique.
9	Pipelined DES (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	Loop unrolling pipeline method is used for improving performance of DES Algorithm. Established DES algorithm of Iterative method creates 64bit cryptograph after each 16 clock, on the other hand, in case using pipeline method creates 64 bit cryptograph each clock after 16 clock.
10	MD5 hash Algorithm (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	MD5 algorithm is a transformation of modified MD4 algorithm. That is, MD5 algorithm is taken over general idea of MD4 algorithm. Basic concept is hashing is supposed to be a unit of block such as encryption
11	HMAC-MD5 hash algorithms (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	It output 128bit's hash result data about 160bit's key data as input in HMAC-MD5 algorithm. At this time, input data is inputed several times, and then it performs data into 512 units internally.
12	Pipelined 3DES (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	3DES is consisted of three DES blocks. After passing through each DES block successively, the final 3DES result is output.
13	High-speed ECC (Soft IP / Verilog)	Anyang University (http://www.anyang.ac.kr)	Processor & Micro-controller 〉Crypto Processor	Main merit of ECC is using much smaller Key as well as having the same safety compared to other encryption systems.
14	FG70A_A_GENERIC_CORE: 0.45um Gate Array (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Physical Library 〉I/O 〉Connectivity I/O	UMC's 0.45um 5V 1P3M Logic Process Raw gate density: 7,870 gates/square millimeter offers high density needed for low cost performance Wide drive strength range and optimized P/N ratio for performance
15	FXPORC030HA0A: Power-On Reset (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉Power On Reset	UMC 0.18um 1.8V 1P6M logic process Operating voltage range: 1.4V ~ 2.2V Operating junction temp. range: -40degC ~ 125degC
16	PLLA010: Phase-Locked Loop (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉PLL/DLL	Low jitter clock output , Generic PLL , Pure 1.8V power supply, 6-bit programmable pre-divider, 6-bit programmable loop-divider, Built-in isolated PLL testing circuit
17	OSC8005: RC-Oscillator (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉Oscillator	UMC 0.35um 3.3V 1P5M logic process, Oscillating frequency tunable by the external resistor: 15~50 MHz Low power supply current, Oscillator enable/disable pin provided

2005년 1월부터 2월 초까지 465개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 30개 IP의 정보를 제공해 드리며,
SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total : 1385개)

No.	IP Name (Type / Format)	Seller	Category	Description
18	VDT9001: Voltage Detector (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 Others	Built-in high-stability reference source Built-in hysteresis characteristic Supply glitch immunity
19	FXBG030HA0A: Bandgap Voltage Reference (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 Voltage Reference	UMC 0.18um 1.8V 1P6M logic process, Operating voltage range: 1.2V ~ 4.0V, High power supply rejection ratio, Low temperature coefficient, Low process variation effect, Low current dissipation
20	FXDLL311HC0H: Input 100M-200M Hz, output 100M-200M Hz, DDR DLL (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 PLL/DLL	UMC 0.13um 1.2V 1P8M logic process, DDR SDRAM controller usage, Four channels with 20% DQS delay, Low jitter output, No external component required
21	FXADDA185H90A: 18 bit 96KHz Sigma-Delta audio Codec (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 Coder/Decoder(CODEC)	90-dB SNR sigma-delta DAC, 92-dB SNR sigma-delta ADC, Support audio sampling rates: 8kHz - 96kHz, Digital interpolation filter, De-emphasis filter supports for 44.1kHz, 32kHz, 48kHz
22	FXDAC162HA0A: 16 bit 96KSPS voltage output stereo-line DAC (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 Converter 〉 DAC	90-dB SNR sigma-delta DAC, Built-in anti pop sound circuit, Built-in ESD protection, Serial & Parallel DAI (digital audio interface) supported both in Master & Slave, Low Clock Jitter Sensitivity, Stereo-Line Outputs

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23	REG9002H: Voltage Regulator (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Analog & Mixed Signal 〉 Regulator	UMC 0.25um 3.3V 1P5M logic process, High current driving capability, Low dropout voltage, Low stand-by current, High line regulation, High load regulation
24	FXFEP160H90A: 2.5V 10/100BASE-TX Fast Ethernet Analog PHY (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Networking 〉Protocol Layer 〉 Ethernet	UMC advanced 0.25um 2.5V 1P5M standard logic process, IEEE 802.3, 802.3u compliant, FDDI-TP-PMD compliant capabilities, Full-duplex and half-duplex
25	FTWDT010: WatchDog Timer (Soft IP / VHDL, Verilog)	Faraday Technology Corporation (http://www.faraday-tech.com)	Peripheral Core 〉Timer / Watchdog	Speed: 66MHz APB Clock Rate Support, On timeout, outputs one or a combination of system reset, system interrupt and external interrupt, 32-bit down counter, Internal or external clock source
26	FTDDR020_S: DDR Memory Controller (Soft IP / VHDL, Verilog)	Faraday Technology Corporation (http://www.faraday-tech.com)	Peripheral Core 〉 Controller 〉Memory Controller	AMBA AHB 2.0 compliant, Rich DDR RAM type support, Use burst length of 4 to speed up the read /write cycle, Programmable refresh type (staggered or non-staggered)
27	FSC0U_D_SH: 0.13um Synchronous Fusion High Density Single Port Static RAM (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Memory Element 〉 Synchronous SRAM	Synchronous read and write operations Low leakage device-based design, with HS devices on critical path Full custom layout density per customer configuration
28	FS70A_B_SD: 0.5um Synchronous Diffusion Programmable ROM Compiler (Hard IP / GDS II)	Faraday Technology Corporation (http://www.faraday-tech.com)	Memory Element 〉 Synchronous ROM	Compatible with UMC's 0.5um 5V 1P2M logic process, Synchronous read operation, One (1) read address port, Diffusion programmable, Fully customized layout density
29	FS70A_B_RC: 0.5um Asynchronous Contact Programmable ROM (Hard IP / GDSII)	Faraday Technology Corporation (http://www.faraday-tech.com)	Memory Element 〉 Asynchronous ROM	Contact programmable to obtain fast TAT, Fully customized layout density, Fully static operation, no operating power consumption in both standby and power down modes
30	TL6510AD (Hard IP / GDS II)	TLi Inc. (http://www.tli.co.kr)	Analog & Mixed Signal 〉 Converter 〉 ADC	10bit 5Msps Pipeline ADC. Operating Voltage without SNDR degration is 2.6~3.6V. Input range is 2Vpp with on-chip reference. SNDR at fin=100kHz, fs=5MHz is 60dB typically. Consumes less than 3mA at 3V. Core size is ~1mm2. Supports Nyquist Input frequency.