Design of Reflector Type Frequency Doubler for Undesired Harmonic Suppression Using Harmonic Load Pull Simulation Technique

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Abstract

In this paper, a study on the reflector type frequency doubler, to suppress the undesired harmonics, is presented. A 12 to 24 GHz reflective frequency doubler is simulated and experimented. Design procedure of the frequency doubler with reflector is provided and the frequency doubler with good spectral purity is fabricated successfully. It has harmonic suppression of the 40~50 dBc in the 1st harmonic and the 50~60 dBc in the 3rd harmonic with no additional filter. And, it has conversion gain with the input power of 0 dBm over bandwidth of 500 MHz. A NEC's ne71300(N) GaAs FET is used and the nonlinear model(EEFET3) using IC-CAP program is extracted for harmonic load pull simulation. Good agreement between simulated and measured results has been achieved.

Key words : Frequency Multiplier, Reflector, Frequency Doubler, Harmonic Load Pull Simulation.

I. Introduction

The frequency multiplier is available for many electronic systems in the microwave and mm-wave frequency ranges. Specially, it is used to extend the upper frequency limit of oscillation in communication system. Therefore, a frequency multiplication of a frequency source with a low phase noise such as a PLL(Phased Locked Loop), is a preferred solution by radio manufacturers to generate a high frequency source(Fig. 1).

Among many frequency multiplier design topologies, the reflector provides the better gain and the lower spurious[1]~[7]. This topology was proposed first by Rauscher[1] and then was applied by other researchers[2]~[7]. Their main interest is not suppression for the undesired harmonic but a little improvement for a conversion gain. To construct the effective radio frequency system, appropriate suppression for undesired harmonic is very important. In this paper, a detailed reflective frequency multiplier design procedure is described and suppression performance for the undesired harmonic is improved using harmonic load pull simulation technique.

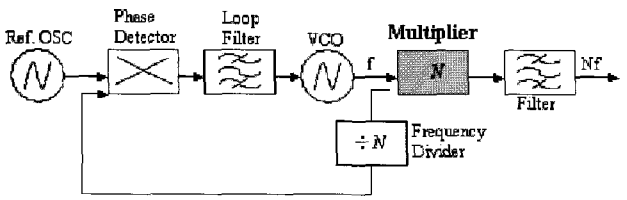

Fig. 1. Generation of a signal with low phase noise using PLL and frequency multiplier.

To perform harmonic load pull simulation, a nonlinear model is needed. A FET nonlinear model is extracted using ICCAP program. A simulation result used an extracted nonlinear model has a good expectation of the conversion gain and undesired harmonic suppression characteristics.

II. Nonlinear MESFET Model

A nonlinear model of a FET is used to predict the performance of nonlinear components in many cases. In contrast to the operation of power amplifier and oscillator, which may be visualized as an essentially linear circuit problem perturbed by nonlinear effects, frequency multiplier relies on nonlinear device behavior as the basic operation mechanism[1]. Therefore, an accurate nonlinear model for the frequency multiplier design is more effective. The object of the nonlinear modeling is not to propose of the new channel current model but to predict a nonlinear characteristic of the multiplier accurately.

The general nonlinear equivalent circuit of a FET is given in Fig. 2(a)[8]. The entire nonlinear model is divided in intrinsic and extrinsic model.

The extrinsic model parameters such as $L_g, L_d, L_s, R_g, R_d, R_s, C_{pg}, C_{pd}$ induced from wire bonding and pad parasitic can be extracted from DC characteristics of a FET or from RF characteristics using a cold FET method. And the intrinsic model parameters such as C_{gs}, C_{ds}, C_{gd},

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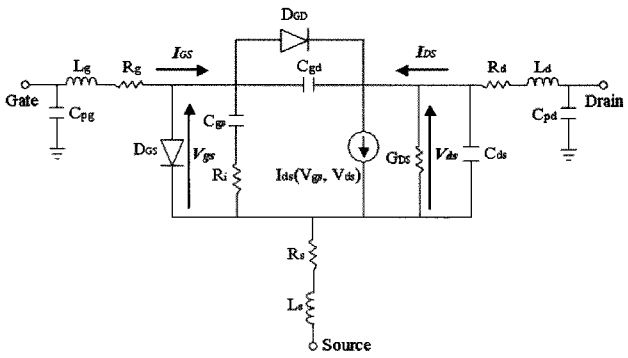
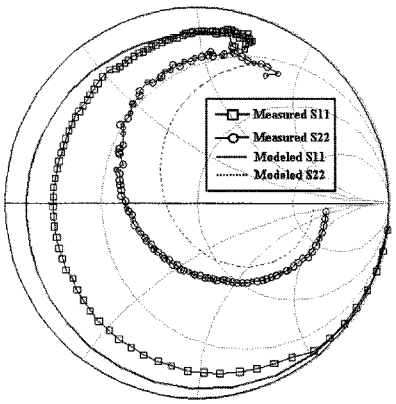
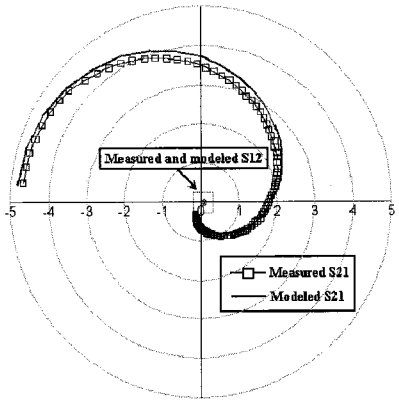


Extrinsic model parameter			Intrinsic model parameter		
Name	Value	Unit	Name	Value	Unit
Lg	235	pH	Vto	−1.091	V
Ls	10	pH	Gamma	4.188m	1/V
Ld	397	pH	Kapa	33.33m	1/V
Cpg	7	fF	Peff	695.6m	W
Cpd	1	fF	Cdso	88.98f	F
Rg	1.4	Ohms	Kapaac	76.0m	1/V
Rs	5.563	Ohms	Peffac	1.3	W
Rd	1.4	Ohms	Lambda	80.98	1/V

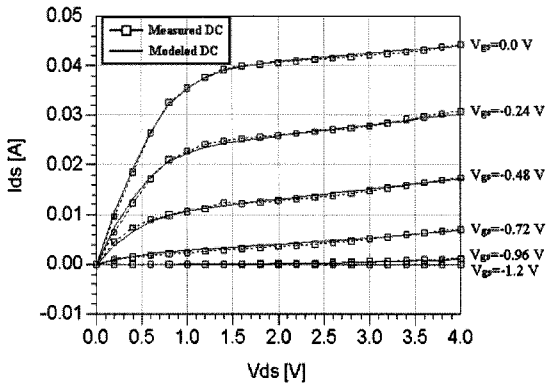
(a) An equivalent circuit for a FET nonlinear model and extracted parameters



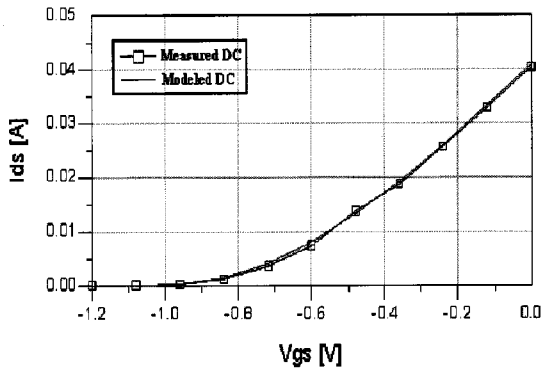
(b) Smith chart plot of the S_{11} and S_{22} characteristic



(c) Polar plot of the S_{12} and S_{21} characteristic



(d) V_{ds}-I_{ds} curve



(e) V_{gs}-I_{ds} curve at V_{ds}=3 V

Fig. 2. Extraction and verification of the nonlinear model for the ne71300(N) GaAs FET.

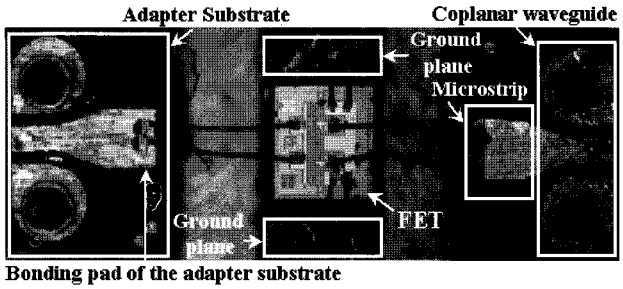


Fig. 3. DUT setup with adapter substrate for CPW to microstrip transition.

R_i, g_m, g_d can be extracted by Dambrine's method which is related the intrinsic parameters to the equations in the form of Y parameters that are transformed from measured S parameters of the device after de-embedding the extrinsic parameters.

In this nonlinear model extraction, the difference from normal modeling that is offered by the chip manufacturer is to contain a wire bonding effect in calibration and AC measurement. While calibrated based on the DUT(Device Under Test) setup in the Fig. 3, a special calibration substrate requires moving reference plane up

to the bonding pad of the adapter substrates. Another merit of this DUT is that it is possible to measure even not to probe a chip directly using general probe tip that has a CPW(Ground-Signal-Ground) form.

A nonlinear model extraction was tried using the agilent ICCAP(Integrated Circuits Characterization and Analysis Program) that is the commercial program for chip modeling. And the EEFET3(EEHEMT1) empirical analytic model that is known accurate relatively and offered by ICCAP is selected. A fundamental setup for a measurement such as frequency ranges, a power value and a bias sweeping is installed by workstation where ICCAP program is contained. In this, it has a frequency range from 0.5 to 40 GHz, input power of 10 dBm, V_{ds} from 0.0 to 4.0 V and V_{gs} from −1.2 to 0.0 V. DC and AC data that need to extract nonlinear model was measured based on this setting. The model can be automated with extraction macros, or the parameters can be extracted individually from the measured data.

Extracted intrinsic and extrinsic parameters are given in Fig. 2(a) and only more important parameters in intrinsic case are contained. Extrinsic parameters have a large value relatively due to the wire bonding effect. A DUT contains two wires of 500 um in gate and drain, respectively, and four wires of 100 um in source. The measured and extracted AC and DC data are shown in Figs. 2(b)&(c), in Figs. 2(d)&(e), respectively. The extracted S_{11}, S_{22} have some difference from the measured data but other AC and DC modeled parameters with an exception of these parameters have a good identity from the measured data. The frequency doubler which is fabricated is shown in Fig. 4. Gate and drain bias voltage is injected through the yellow and red line, respectively. Detailed bias condition is reported in chapter Ⅳ.

Ⅲ. Basic Theory & Analysis of the Frequency Reflector

As mentioned, a main role of the reflector is related to the improvement in conversion gain and the suppression for undesired harmonic. The description below would be valuable to explain two functions of the reflector[9],[10].

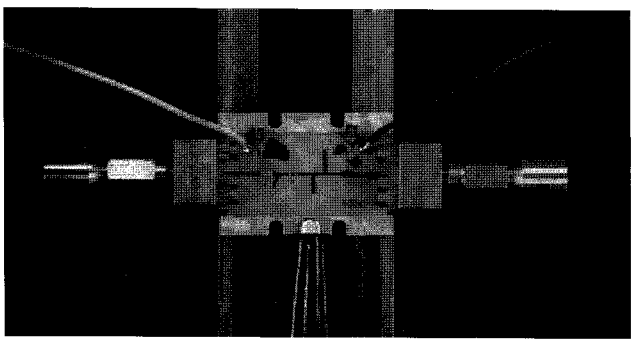


Fig. 4. 12 GHz to 24 GHz frequency doubler.

Assuming the harmonics fed back to the input port are of a lower level than the fundamental signal power, P_o, the following mechanisms contribute to enhance the output power at the desired harmonic: power amplification of the output harmonic(n) and frequency conversion by mixing the $(n-1)$ and $(n+1)$ output harmonics with the fundamental frequency. So, the power at the desired n^{th} harmonic, P_n, can be represented by

$$P_n=(1-A_n)[P_1\times MG+P_nA_n\times G_n+ (P_{n-1}A_{n-1}+P_{n+1}A_{n+1})\times CG] + \text{other terms} \quad (1)$$

where

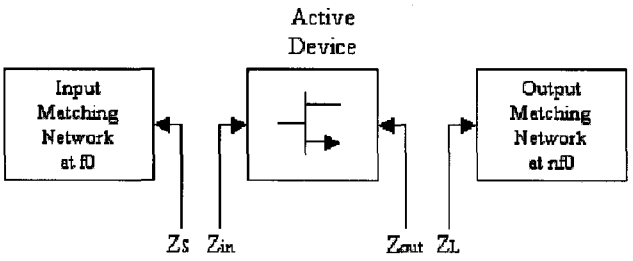
P_n is the output power at nth harmonic,
P_1 is the output power at fundamental frequency, f_1,
P_{n-1}, P_{n+1} are the power at the harmonics $(n-1)$, $(n+1)$, respectively,
A_{n-1}, A_{n+1} are the power coupling or reflection coefficient at the harmonics $(n-1)$, $(n+1)$, respectively, and
MG, CG are the multiplication gain and conversion gain respectively.

In this equation, one can identify the three most important mechanisms contributing to the general multiplication efficiency.

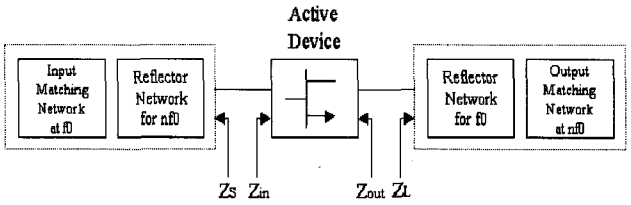
They are (a) frequency multiplication from the fundamental frequency to the n^{th} harmonic, whose power gain is defined by MG; (b) large-signal amplification of part of the n^{th} harmonic fed back to the input with a power gain G_n; (c) frequency conversion resulting from mixing the fundamental frequency with the feedback harmonics $(n-1)$ and $(n+1)$ with a conversion gain denoted by CG.

Using the above-mentioned concept, reflector can be used to a get high general multiplication gain in a frequency multiplier design. Frequency multiplier diagram with and without reflector is showed in Fig. 5. It is reported to get improvement by several dB in a conversion gain using this design method[5]. But, the rejection of the unwanted harmonic is not as great as desired in many cases although this is a important criterion to determine the performance of the frequency multiplier in microwave and mm-wave system. Practical design procedure in reflector for suppression of the undesired harmonic would be presented in chapter Ⅳ.

Frequency reflector can be implemented easily like in Fig. 6. In the doubler case, a quarter-wave open stub in



(a) Conventional frequency multiplier



(b) Frequency multiplier containing reflector network

Fig. 5. Frequency multiplier block diagram.

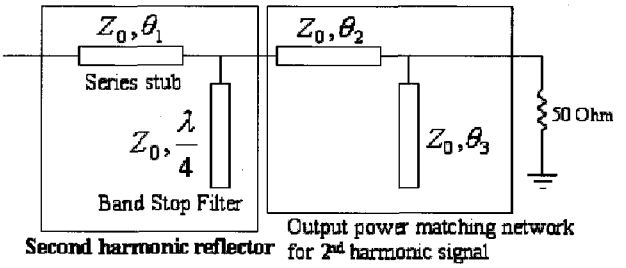


Fig. 6. Reflective matching design in doubler[11].

the fundamental frequency plays a role of the band stop filter for 1st and 3rd harmonic. Fundamental and third harmonic is short circuit and second harmonic is open circuit in the point meeting series stub and quarter-wave open stub. Therefore, 1st and 3rd harmonic is rejected but 2nd harmonic passes without a loss ideally after this structure. As it is shown in Fig. 6, four design parameters that are open stub length, θ_1, θ_2 and θ_3 exist. Optimum harmonic suppression can be obtained by controlling an open stub length and an optimum conversion gain by controlling θ_1, θ_2 and θ_3.

The basic design concept concerns a load condition and it affects input impedance. Since the fundamental frequency component appearing at the drain is reflected at the junction in the multiplier's output circuit, the electrical length between the FET drain and the junction largely affects conversion efficiency. This theory can be proved through the equations from (2) to (6). In bias case of the class B, the peak current I_{peak} and the second harmonic drain current I_{d2} is defined in equations (2) and (3), respectively. Where I_{dss} is current when V_{gs} is zero, V_p is pinch-off voltage, V_{Go} is operating voltage of the input voltage sinusoidal signal and V_g is the gate voltage.

$$I_{peak} = I_{dss}(V_p - V_{G0} + V_g)/V_p \tag{2}$$

$$I_{d2} = \frac{2I_{peak}}{3\pi} \tag{3}$$

An input power at the fundamental frequency $P_{in}(f_1)$ and a conversion gain can be defined in equations (4) and (5), respectively.

$$P_{in}(f_1) = R_{in}|I_g|^2 = \frac{R_{in}|V_g|^2}{|Z_{in}|^2} \tag{4}$$

$$\text{Conversion gain} = \frac{P_{out}(f_2)}{P_{in}(f_1)} = \frac{R_L|I_{d2}|^2}{P_{in}(f_1)} \tag{5}$$

$$\text{Conversion gain} \propto \frac{R_L G_{M0}^2 |Z_{in}|^2}{R_{in}} \tag{6}$$

$$\text{Conversion gain} \propto \frac{R_L G_{M0}^2 (R_{in}^2 + X_{in}^2)}{R_{in}} \tag{7}$$

where $P_{out}(f_2)$ is the second harmonic output power, I_g is the gate current, Z_{in} is the input impedance, R_{in} is the real part of Z_{in}, R_L is the load resistance and G_{M0} is the transconductance that is defined absolute value of the $\frac{I_{d2}}{V_g}$.

Equations (6) and (7) can be obtained from the relation between the equations (4) and (5). This equation shows that the conversion gain can be roughly affected by the equivalent input impedance of the circuit. Especially, a conversion gain is affected by reactance value of the input impedance largely.

As shown in Fig. 7, there is a large variation of the conversion gain as the function of the series stub length. And, it can be seen that the conversion gain and imaginary value of the input impedance have similar shape. Although multiplier designers use a quarter-wave open stub frequently to get a good spectral performance easily, the detailed design is required due to the large variation of the conversion gain as a function of the series stub length.

The main roles of the reflector network are summarized as follows.

(a) The quarter wave open stub of the fundamental frequency has a role of the band stop filter for first and third harmonic.

(b) By controlling a series stub length, a multiplication gain can be improved or degraded by a few or several dB.

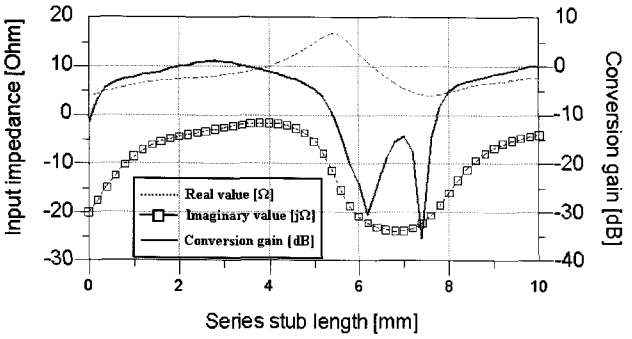


Fig. 7. Input impedance and conversion gain variation as a function of the series stub length.

(c) It is possible to match for the second harmonic by using double open stub.

Ⅳ. Reflector Design Using Harmonic Load Pull Simulation Technique

Harmonic load pull simulation method is used to construct the reflector network for the suppression of the undesired harmonic. In Fig. 6, there are four variables affecting the performance of the multiplier. The main consideration in a design is the optimization for these design parameters. The detailed design procedure is as follows.

Step 1. Selection of the harmonic optimum load impedance and a design of the harmonic matching

The circuit schematic for the harmonic load pull simulation is shown in Fig. 8. A lot of available information that is important in a frequency doubler design can be obtained from this simulation procedure. Design parameters such as a fundamental source and harmonic load optimum matching point, an optimum bias condition, a conversion gain, a harmonic power, a harmonic PAE(Power Added Efficiency) and a thermal dissipation can be calculated from the proper variable establishment and the optimization design method.

Optimum load impedance is illustrated up to the third harmonic in Fig. 9. If this point is not in an unstable region, the optimum matching point can be selected. Based on the harmonic load pull simulation result, matching for second harmonic can be designed. Entire multiplier efficiency can be taken an aim roughly in this step, although this simulation has some difference from final simulation due to the use of some ideal passive circuit such as a matching, a DC block and a DC feed line in a simulation schematic of the Fig. 8. Several important simulation results are given in Table 1.

A harmonic suppression performance is not good because it does not contain a reflector structure. It is difficult to get good a spectral performance using only second harmonic matching design.

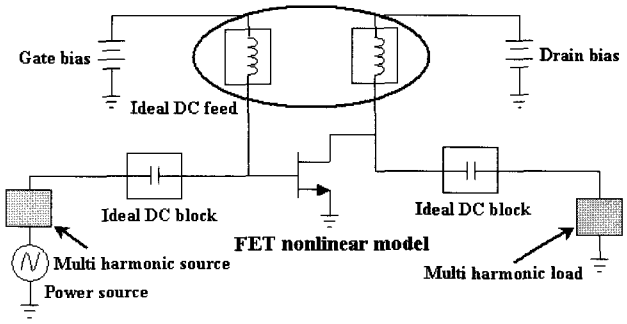


Fig. 8. The circuit schematic for the harmonic load pull simulation.

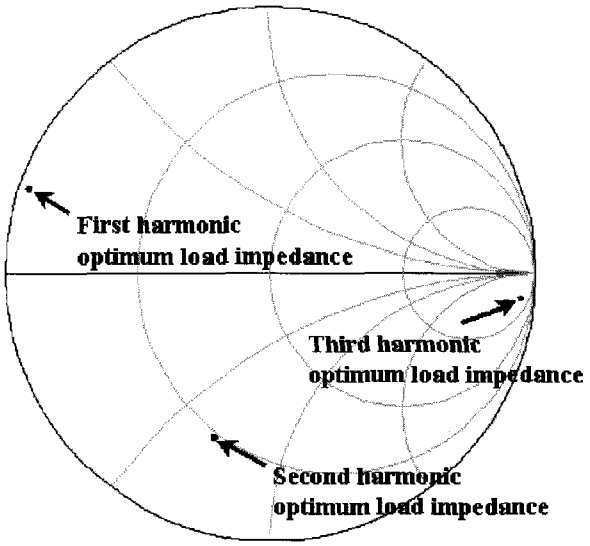


Fig. 9. Smith chart diagram up to the third harmonic optimum impedance.

Table 1. Simulation results after optimization.

Optimization object		Optimization value
Bias condition		V_{ds}=2.5 V, V_{gs}=0.034 V (I_{dss}bias)
Harmonic suppression	1st	8.042 dBc
	3rd	29.232 dBc
2nd harmonic power		13.039 dBm
Conversion gain		3.094 dB
2nd harmonic PAE		9.718 %

Step 2. Calculation of the open stub performance for the optimum harmonic suppression

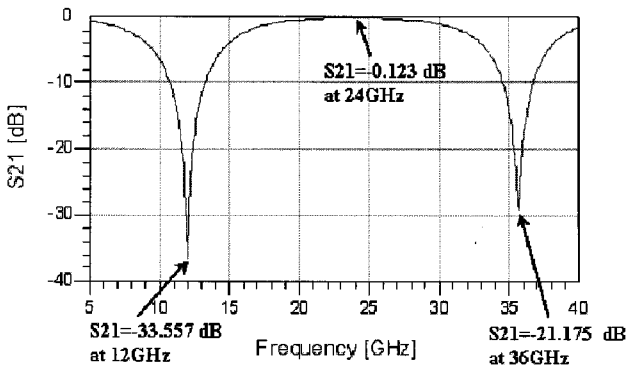


Fig. 10. Performance of harmonic suppression filter using quarter-wave open stub.

In this, the fundamental frequency is a 12 GHz and a design goal is to have low loss for second harmonic. A quarter-wave open stub at the fundamental frequency has a major role for suppression of the undesired harmonic. A simulation of the quarter-wave open stub in Fig. 10 shows narrow bandwidth. But this has good performance as a band stop filter. The operating principle as a the filter of this open stub was explained in Section Ⅲ.

Step 3. Selection of the optimum series stub length for a good conversion gain

And then a conversion gain effect of a series stub length should be checked because it affects a conversion gain largely as illustrated in Fig. 7. This result can be obtained to simulate a variation of the conversion gain as a function of the series stub length. The effect for the conversion gain of the series stub length was already proved in section Ⅲ. From this simulation, we can get information about an optimum series stub length θ_1 for the better conversion gain.

Based on the information for harmonic matching that is given in above steps, matching can be designed. An output matching structure is designed as shown in Fig. 6, considering an optimum 2nd harmonic matching point in step 1, an open stub length for the harmonic suppression in step 2, a series stub length in step 3. It is important to match to the optimum load impedance maintaining a proper open stub length to suppress for the undesired harmonic sufficiently.

A series capacitor would be used to block the DC bias applied to a FET as well as a low frequency signal while allowing the RF signal to pass through with a minimum loss. Although thin film capacitor that is used in this has a good performance and small size, the loss increases in higher frequency than 18 GHz. So, this capacitor was used only for an input DC block. An output DC block was implemented using a parallel-coupled line. These DC blocks have a pass loss less than 0.3 dB.

Step 4. An output matching design for the harmonic suppression and a passive circuit design

In order to feed a bias voltage to the transistor, a DC feed network is required. When designing this element, it is important that RF characteristics of a circuit should be maintained whether a DC feed is connected to the circuit or not. Also, a signal should not be flown to the power supply through DC feed. These two considerations lead us to design DC feed network using a form of low pass filter. And the length of the microstrip line is typically a quarter-wave length at the mid band frequency in order to make very high impedance at the connected point between the matching network and the DC feed.

These passive circuits are simulated using momentum method. It is stored as the form of the dataset and entire circuit containing an active device is finally simulated to predict performance of the multiplier. Because, an ideal passive circuit as in Fig. 8 is substituted a non-ideal circuit, the simulation performance degrades than expected result in step 1. The detailed simulation and experiment results are given in chapter Ⅴ.

Ⅴ. Simulation & Experiment Results And Discussion

To predict a performance of the nonlinear component accurately, harmonic load pull simulation is used[10],[12]. A nonlinear model must be required in this simulation and the accuracy in a nonlinear model determines the identity between simulation and experiment. The extracted nonlinear model is used as explained in chapter Ⅱ.

5-1 Simulation and Experiment Results

The measured result of the conversion gain is compared with simulations as shown in Fig. 11. The experiment results show a good agreement with simulation having the difference less than 2 dB in an available input power range, but have a larger gap for the high input power due to the inaccurate prediction in a large signal injection. It is found to have a conversion gain when an input power is from 0 dBm to 4 dBm.

The output power as a function of an input power is reported in Fig. 12. The reflective doubler has an additional rejection of 20~30 dBc for a 1st and 3rd spurious harmonic compared to the conventional case. Fig. 12 shows the reflector can be an effective design method of the frequency doubler with the low spurious.

Measured and simulated output power versus input fre-

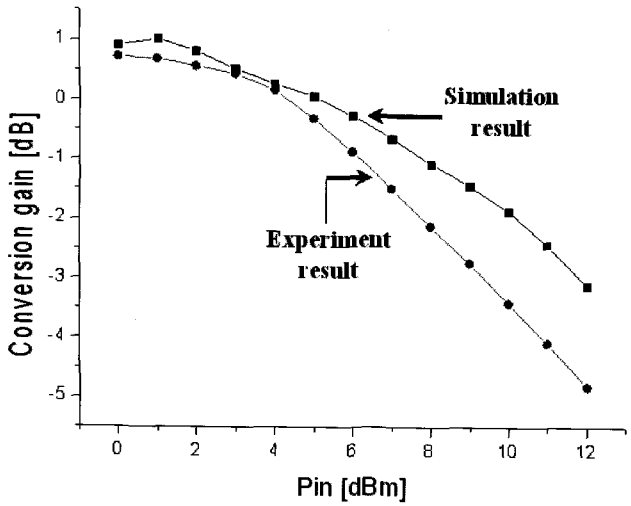
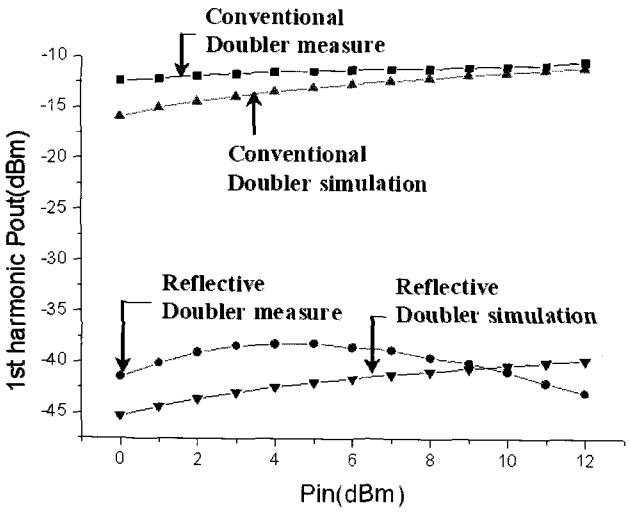
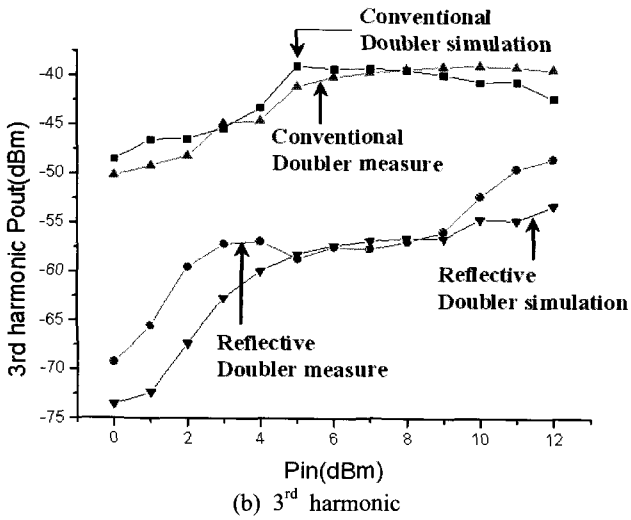


Fig. 11. The conversion gain of 2nd harmonic as a function of the input power.



(a) 1st harmonic



(b) 3rd harmonic

Fig. 12. Comparison of the output power for the conventional and reflective doubler.

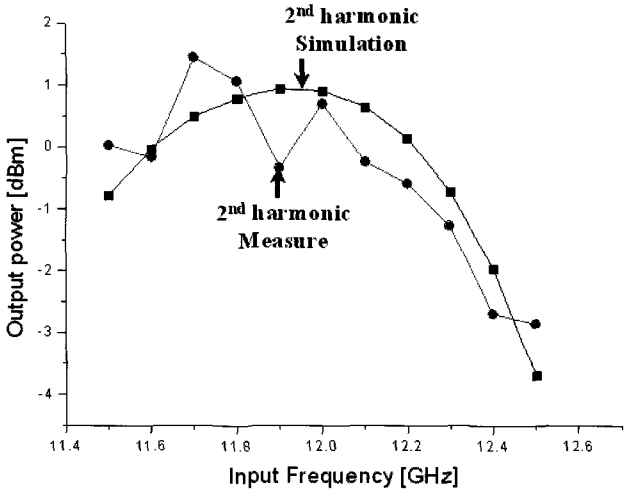


Fig. 13. Measured and simulated output power versus input frequency(input power=0 dBm).

quency at the input power of 0 dBm is shown in Fig. 13. It has a low conversion gain relatively at the higher frequency than 12 GHz that is design frequency.

5-2 Discussion

Reflective frequency doubler has a good harmonic suppression compared to the conventional design. It has a proper conversion gain in operating frequency. But, a better conversion gain can't be obtained due to the chip feature that has a low gain in K-band. Some difference between simulation results and measured data is thought due to the nonlinear model inaccuracy but its difference is acceptable. An accurate nonlinear model is another frequency multiplier design key. A suppression design method for the unused harmonic proposed in this will give RF system engineers much flexibility.

Ⅵ. Conclusion

Reflector network is successfully applied to the frequency doubler operated in K band, and it is proved undesired harmonic suppression using reflector an effective solution using simulation and experiment successfully. A reflective frequency multiplier design procedure is presented using harmonic load pull simulation. Specially, the reflective doubler in this has a higher harmonic suppression than conventional doublers in other papers. It has harmonic suppression of the 40~50 dBc in the 1st harmonic and the 50~70 dBc in the 3rd harmonic.

Therefore, the frequency chain for the frequency source with a low phase horse in a RF system can be implemented using filter less than a conventional case. And, it is helpful to make the frequency synthesizer to be simplified.

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