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Power-aware Test Framework for NoC(Network-on-Chip)

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NoC에서의 저전력 테스트 구조

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Abstract In this paper, we propose the power-aware test framework for Network-on-Chip, which is based on embedded processor and on-chip network. First, the possibility of using embedded processor and on-chip network isintroduced and evaluated with benchmark system to test the other embeddedcores. And second, a new generation method of test pattern is presented to reduce the power consumption of on-chip network, which is called don't care mapping. The experimental results show that the embedded processor can be executed like the automatic test equipments, and the test time is reduced and the power consumption is reduced up to 8% at the communication components.

요 약 본 논문에서는 임베디드 프로세서 및 네트워크 구조를 기반으로 구성된 NoC(Network-On-Chip)의 저전력 테스트 구조를 제안한다. 임베디드 프로세서와 여러개의 코어로 구성된 네트워크 구조에 벤치마크 회로를 직접 연결하여 테스트 전력소모를 평가하였으며, 각 코어의 테스트 패턴을 저전력 소모가 되도록 매핑하여 테스트 전력소모를 감소시켰다. 또한 임베디드 프로세스 코어를 ATE(Automatic Test Equipment)로 사용하여 테스트 시간을 줄일수 있었다. ISCAS89 벤치마크 회로에 대해서 테스트 시간은 매우 효과적으로 감소되었으며 평균 전력소모는 약 8%가 감소되었다.

Keywords: Test, Network-on-Chip, TAM, Low-power

1. Introduction

Modern SoC (System-on-Chip) typically contain dozens of IP (Intellectual Property) cores. Especially, such systems requirecommunication templates with several dozens of Gbits/s of bandwidth, which must be also reusable to meet time-to-market requirements. To provide reusability, scalability, high bandwidth and low latency, the Network-on-Chip (NoC) design paradigm has recently proposed as an alternative to traditional broadcast and shared-bus architectures for core-based systems [1]. A study presented in [2] shows that NoCs have better communication performance than conventional bus architectures. Therefore, it is clear that NoCs can potentially become the preferred interconnection approach for SoCs being developed in a near future [3].

However, the growing design complexity of chips, device size miniaturization, increasing transistor count, and high clock frequencies have led to a dramatic increase in the number of possible fault sites and fault types [4]. Consequently, a high test data volume is needed for high-quality testing. However, the high test data volume leads to long testing timesand large memory size.

In addition, the design of test access mechanism (TAM) is one of main issues to testing dozens of embedded cores in the NoC. However, the NoC testing implies much power consumption, since the embedded cores in NoC can be tested in parallel, and just then the cores, routers and channels are activate at the same time. Therefore, a new method for the low-power consumption during NoC test is necessary to ensure the safeness of the

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testing.

This paper proposes the power-aware test framework for NoC, which is based on embedded process and on-chip network. First, the possibility of using embedded processor and on-chip network is introduced and evaluated with benchmark system to test the other cores. And second, a new generation method of test pattern is presented to reduce the power consumption of on-chip network, which is called don't care mapping. The experimental results show that the embedded processor can be executed like the automatic test equipment (ATE), and the power consumption is reduced up to 8% at the communication components.

This paper is organized as follows: Section 2 reviews some related works and explains our motivations of the proposed method. In section 3, our proposed method is explained in detail. Section 4 introduces a case study with some experimental results. Section 6 concludes this paper.

2. Related Works and Motivations

Until recent years, many efficient TAM architectures are proposed for DFT (Design for Testability). These are grouped into three main categories in [5]: multiplexing [6], serial connection [7] and bus-based connection [8]. In these cases, the ATE and the ATE interface are additionally required for the TAM as shown in Fig. 1, and test patterns are applied through ATE. According to the literature [9], ATE cost is a significant part of the overall cost of manufacturing test, and is governed by speed and timing accuracy, performance, the number of pins, memory depth and special functionality for mixed signal and RF cores. Complex SoCs, which have higher pin counts and test data volume to attain high fault coverage at each embedded cores, require an expensive external ATE.

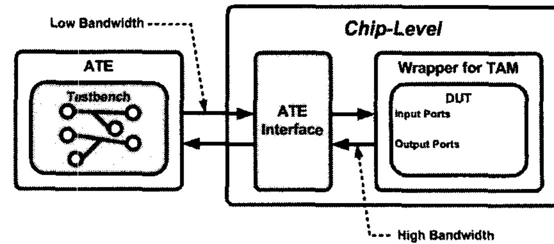

Figure 1. Automatic test environment through TAM.

With the introduction of NoC, valuable works have been proposed for embedded core testing based on this new architecture. In [5], a TAM architecture based on a packet switching communication is presented. The proposed model, called NIMA, is defined to allow modularity, generality, and configurability for the test architecture. In [10], the authors extended the results of a previous on-chip network research [3] to a test scheduling algorithm with power constraints considered. A new test data transportation method is proposed using multiple data flit formats in [11]. With this method, a data flit can contain multiples bits for each wrapper scan chain, instead of only 1 bit/chain in traditional test application methods.

However, these approaches mainly considered how to support embedded core testing using the on-chip network. One major problem of these literatures is that the external ATE with low-bandwidth cannot control easily the test procedure in both the cores and on-chip network. Recently, in [12-15], they proposed a test platform for embedded processor based system-on-chip (SoC). In these cases, the embedded processor is employed as a controllable ATE to execute the test programs for all the other embedded cores through system bus in SoC. In this paper, we extend this method to a NoC with communication protocols and functional wrappers already well-defined.

Recently, the increasing dominance of the power consumption of these on-chip networks in present day systems, poses critical challenges that need to be address lest they become a bottleneck in the development of high performance systems [16]. The power consumption in the routers and the links of the Alpha 21364 microprocessor

were found to be about 20% of the total power consumption [17]. In the MIT Raw on-chip network, the network components constitute 36% of the total power consumption [18]. In [19], the authors explained that these numbers indicate the significance of managing the interconnect power consumption.

Nevertheless, present most literatures [3, 10, and 20] have focused on the test schedulingproblem to minimize test application time under power constraints. In this paper, therefore, we propose new approach to reduce the power consumption of on-chip network during the embedded core testing.

3. The Proposed Test Framework

The overview of proposed framework is illustrated in Fig. 2.There are embedded processor, embedded memory and system bus to execute main program in general SoC platform. It is very likely that there is main PE (processing element) to manage overall system in NoC architecture. Referencing to the literatures [14, 15], we expand the concept to on-chip communication network. The proposed framework can be grouped to hardware and software parts.

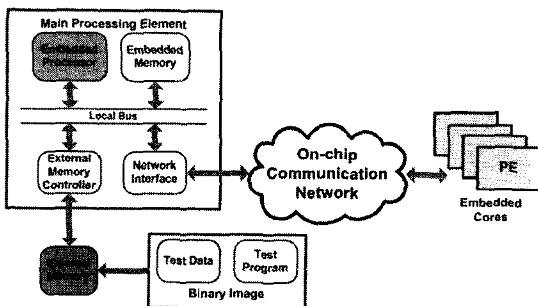

Figure 2. Conceptual overview of the proposed framework based on embedded processor.

The software includes test data and test program, since our proposed methodology is basically a C-based testing. Therefore, we need a test program which is described such as C or C++. After compilation of the test program with test data, the binary image can be loaded into external memory for execution. And, the embedded processor will execute the test program and transfer test pattern to the other embedded cores through network interface.

The hardware is composed of a scan-based core, network interface and TAM controller. Since all packets including functional and test data are send/received through on-chip communication, the test packets are also transferred to core through router and network interface. Only when the status register indicates testing mode, the TAM controller is activated. To compose this architecture effectively, we used IEEE Std. 1500 [21] wrapper to the scan-based core. It is enabled that the hardware overheads and design complexity are minimized.

The total test flow can be decided by software in the proposed framework, but the test data is generated beforehand. We generate the test packet such as Fig. 3 to minimize the power consumption of on-chip network.

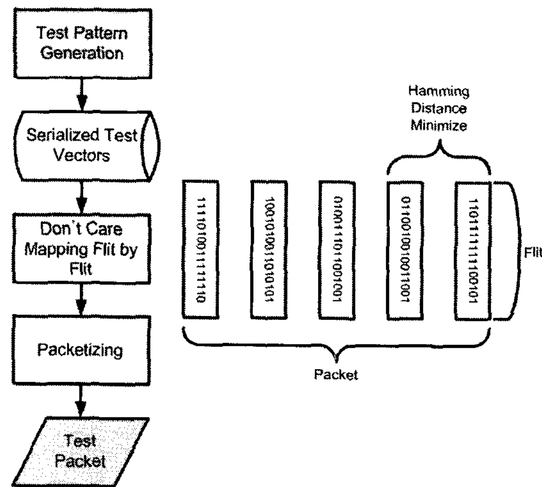

Figure 3. Generation flow of test packet.

In general test pattern for the full scan-based core, there are many don't care bits which have no influence on testing. We mapped these bits to 0 or 1 for minimizing hamming distance between flit and flit. This approach is very useful, because the flit traversesinduce the dynamic power consumption which is the primary source of power

consumed in CMOS circuits.

4. Experimental Results

In this paper we do not use the ITC 2002 SOC test benchmarks [22], because these benchmarks are not suitable to estimate total power consumption of communication components. As shown in Fig. 4, we assume new example system, which is consists of s5378, s9234, s13207, s15850, s38417, s38584 circuit ofISCAS 89 benchmark, and embedded processor. The 7 nodes are organized as a3x3 mesh network, and each router has five physical bidirectional ports (north, south, east, west, and injection/ejection). In this sample system, each core is assumed as a full-scan circuit using the IEEE Std.1500 wrapper.

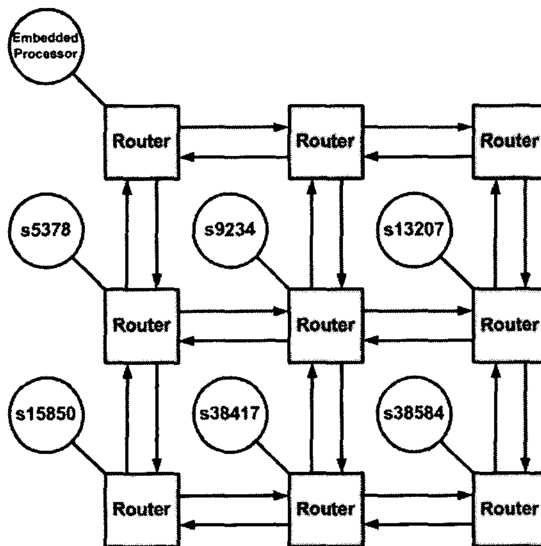

Figure 4. The test system assumed for the simulation.

First of all, we generated test patterns for each core using MinTest ATPG (Automatic Test Pattern Generation) program. This program is based on dynamic compaction method [23] and the patterns have 100% fault coverage. We applied the proposed method to the test patterns for generating the test packets. The Table 1 shows the effectiveness of our methodology when the flit size is 16 bits. At each pattern, the number of switching is decreased average 36 percent compared with 0 mapping.

Table 1. Test packets when the size of flit is 16 bits.

Benchmark	Size of pattern (bits)	Number of switching		Reduction Rate (%)
		0	X	
s5378	23744	5546	3240	41.58
s9234	39264	7928	5247	33.82
s13207	165200	8321	5433	34.71
s15850	76976	8370	5662	32.35
s38417	164736	39326	24631	37.37
s38584	199104	25186	16252	35.47
Average				**35.88**

To evaluate the performance and power consumption of the proposed test framework, we modified Orion [24] and PoPNet [25]. As in [24], we assume an on-chip network with 250MHz frequency, V_{dd} = 1.8V, in 0.18μm process technology. We also fix the router architecture which has 2 VCs (virtual channel) per port, 12 flit input/output buffers per VC, and 1000μm link length. The dimension routing is selected for the network topology, and the propagation delay across data and credit channels is assumed to take a single cycle.

We ran the cycle-accurate simulator about 0, 1 and the proposed don't care mapping when the flit size is 16, 32 and 64 bits. In this case, we assumed that the test packet injection rate of the embedded processor is 0.2 packets per cycle. In the Fig. 5, the performance is improved proportionately with the increasing of channel width. Nevertheless, this performance improvement is not achieved at the expense of higher power consumption, as indicated by the Table 2.

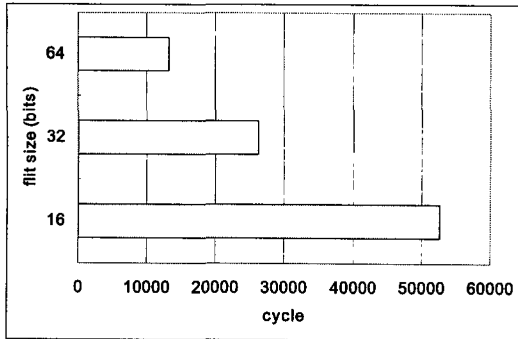

Figure 5. Total simulationcycles of on-chip network.

When we use the external ATE, the speed of test pattern injection is same as the clock speed (about 10 MHz) of ATE.However, if we use the embedded core instead of the external ATE, we can reduce the test time because the injection rate of test pattern is the clock speed of processor (250 MHz).

The Table 2 shows the test time the conventional case(external ATE) and proposed method. The test time of the proposed method is very faster than that of conventional method.

Table 2. Test time in on-chip network

Flit size(bits)	conventional	proposed
16	1.3 ms	52 us
32	2.3 ms	100 us
64	3.5 ms	150 us
Average	2.36 ms	101 us

The Table 3 shows the simulation results of average total power consumption according to mapping methods. We learned that there is little differentiation between 0 and 1 mapping, however the proposed mapping algorithm is showed an about 2% - 8% better average power consumption than 0 or 1 mapping.

Table 3. Average power consumption in on-chip network.

Flit size (bits)	Mapping Method (mW)			Reduction Rate (%)	
	0	1	X	0	1
16	226.16	229.13	221.41	2.10	3.37
32	254.83	258.40	243.87	4.30	5.62
64	305.80	308.85	284.34	7.02	7.94
Average				4.47	5.64

5. Conclusions

In this paper, the power-aware test framework for NoC was proposed, which is based on embedded processor and on-chip network. The experimental results showed that the embedded processor can be executed like the low-cost ATE, and the power consumption can be reduced at the communication components. The main contribution of this paper is the manageable testing through embedded software. And the generation method can be used in the other TAM architectures based on packet-switching network without any modification.

However, our current works excluded a test scheduling algorithm of embedded cores under power constraints. In the near future, we will develop more accurate simulation environment to estimate the power consumption of the embedded cores and on-chip network at the same time.

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