A Low-Power 2.4 GHz CMOS RF Front-End with Temperature Compensation

Yong-Il Kwon[1] · Sangwoon Jung[2] · Hai-Young Lee[2]

Abstract

In this paper, a low-power 2.4 GHz front-end for sensor network application (IEEE 802.15.4 LR-WPAN) is designed in a 0.18 um CMOS process. A power supply circuit with a novel temperature-compensation scheme is presented. The simulation and measurement results show that the front-end (LNA, Mixer) can achieve a voltage gain of 35.3 dB and a noise figure(NF) of 3.1 dB while consuming 5.04 mW (LNA: 2.16 mW, Mixer: 2.88 mW) of power at 27 ℃. The NF includes the loss of BALUN and BPF. The low-IF architecture is used. The voltage gain, noise figure and third-order intercept point (IIP3) variations over −45 ℃ to 85 ℃ are less than 0.2 dB, 0.25 dB and 1.5 dB, respectively.

Key words : Front-End, Temperature Compensation.

Ⅰ. Introduction

A new type of wireless communication with a higher density of nodes and a simple protocol is emerging for low-data-rate distributed sensor network applications such as those used in home automation and industrial systems. Recently, sensors have been developed that can operate from −45 ℃ to 85 ℃ with high reliability and precise RF characteristics. In such a range of environments, sensors with conventional front-end circuit schemes may not provide stable operation due to an increase of the junction leakage current and device-specific characteristic drift[1]. The performance of the front-end circuit is critical to the successful implementation of a receiver. A low-noise amplifier is the first active stage in a receiver system; mixers perform frequency translation by multiplying two signals in the second stage. Therefore, the total noise figure depends on the LNA and the mixer, but particularly on the LNA. An analysis of the noise in cascaded stages can be explained by the Friis equation[2]. Eq. (1) shows the sensitivity as the minimum input signal that yields a given value for the output SNR.

$$P_{in,\min} = -174\ dBm/Hz + NF + 10\log B + SNR_{\min} \quad (1)$$

It can be seen that any variations in the gain or noise of the RF front-end will greatly affect the performance and sensitivity of the entire system noise. This is especially undesirable for those systems with a tight RF budget(e.g. NF, GAIN, and IIP3).

Due to the temperature dependence of the transistor parameters, the performance of a front-end circuit can vary in a large range with the temperature. For a bipolar case, as the transconductance of the transistor is $g_m = Ic/VT$, and VT is proportional to the absolute temperature(PTAT), the performance variation can be offset by biasing the transistor with a PTAT current source[3]. Given that the variation of CMOS transistor g_m depends on the carrier mobility and the threshold voltage, g_m becomes the temperature[4]. Therefore, it is necessary to obtain the temperature characteristics of the CMOS front-end from the simulation results.

In this paper, temperature-compensated biasing for the CMOS front-end circuit is proposed. A variable voltage supply block changes the supply voltage of the front-end circuit to maintain a constant voltage gain and noise figure. Fig. 1 shows a simplified block diagram of the front-end circuit with the temperature compensation scheme. The simulation and measurement results show that the gain of the front-end varies by less than 0.2 dB over the temperature range from −45 ℃ to 85 ℃ while the NF varies by less than 0.25 dB. The following section presents an analysis of the temperature characteristic of devices. Section Ⅲ gives a brief overview of the design of the CMOS front-end with the temperature compensation scheme. The simulation and measurement results of the temperature characteristic of this CMOS front-end are presented in Section Ⅳ. Subsequently, the paper concludes with a summary.

Manuscript received March 22, 2007 ; July 18, 2007. (ID No. 20070322-009J)

[1]SAMSUNG Electro-Mechanics, Central R&D Institute, Suwon, Korea.

[2]Department of Electronics Engineering, Ajou University, Suwon, Korea.

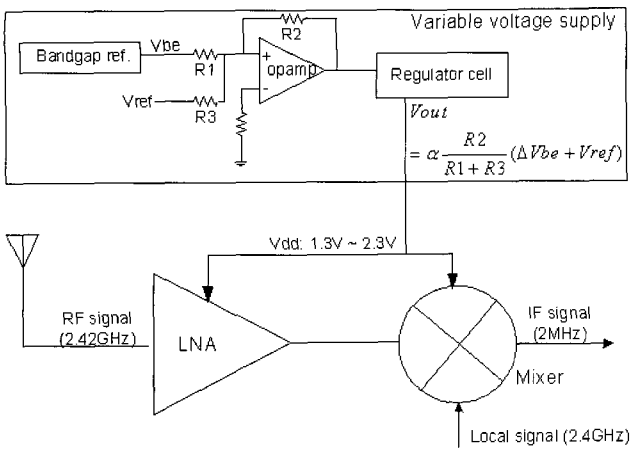


Fig. 1. A block diagram of front-end with temperature compensation scheme.

Ⅱ. Analysis of Temperature Variation

The most common LNA architecture is a single or differential cascade LNA. The MOS version of a cascade LNA is shown in Fig. 2.

With this topology, it is easier to achieve input matching for the power gain and noise figure compared to other circuit topologies[5]. The source degeneration inductor *Ls* is used both to improve the linearity and for input impedance matching. The cascade circuit can reduce the influence of the gate-to-drain overlap capacitance *Cgs* and can improve reverse isolation of the LNA. The input impedance of the amplifier is

$$Z_{in} = s(Ls + Lg) + \frac{1}{sCgs} + \frac{g_{m1}Ls}{Cgs} \tag{2}$$

By tuning the *Ls* and *Lg* to resonate with *Cgs*, the input impedance can achieve 50 Ω. When the input is matched, the entire input stage transconductance is

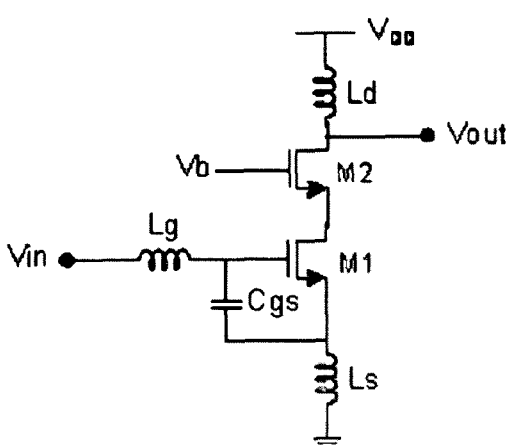


Fig. 2. Cascode LNA circuit.

$$G_m = g_m Q_{in}$$
$$where\ Q_{in} = \frac{1}{Rs}\left(\frac{1}{\omega_0 Cgs}\right) = \frac{1}{Rs}\omega_0(Lg + Ls) \tag{3}$$

Here *Rs* is the source resistance. It is clear that the common source stage gain has been boosted by the *Q* value of the input matching network. The major noise source comes from the thermal noise of input transistor M1. If the gate resistance noise is disregarded through the use of a careful layout, the noise figure can be estimated as

$$NF = 1 + \frac{\gamma}{R_s g_m Q_{in}^2} \tag{4}$$

Here, γ is a biasing-dependent value that is approximately 2 to 3. In CMOS devices, the temperature-dependent effects are mainly due to two factors: the threshold voltage and carrier mobility variations. The threshold voltage has a temperature tendency that is similar to bipolar devices that have a TC-of approximately 2 mV/℃[6]. The carrier mobility will decrease as the temperature increases due to its exponential nature; this will be the dominating variation factor. The fractional temperature coefficient(TC_f) of mobility is simply given by

$$TC_f = \frac{1}{\mu}\frac{\partial \mu(T)}{\partial T} = -1.5T^{-1} \tag{5}$$

Where μ is the mobility of charge carriers and T is absolute temperature. Thus, for a common source stage, the transconductance can be expressed as

$$g_m(T) = \mu(T)C_{ox}\frac{W}{L}(V_{gs} - V_{th}(T)) \tag{6}$$

Where C_{ox} is the gate oxide capacitance per unit area, W is the width of transistor, L is the length of the transistor and V_{th} is the threshold voltage. If constant gate-source voltage biasing is assumed, the TC_f of g_m is then

$$TC_f = \frac{1}{g_m}\frac{\partial g_m(T)}{\partial T} = \frac{1}{\mu}\frac{\partial \mu(T)}{\partial T} \cdot \frac{1}{V_{eff}}\frac{\partial V_{th}(T)}{\partial T}$$
$$= -1.5T^{-1} + \frac{2mV/CENTIGRADE}{V_{eff}} \tag{7}$$

Where $V_{eff} = V_{gs} - V_{th}$ is the overdrive voltage of the common source stage. For a high level of overdrive, the first item will dominate and thus gm will decrease with the temperature in the LNA design if the input network quality factor(Q_{in}) is assumed to be fixed and temperature-independent. It follows from Eq. 3 that the gain of the LNA will then drop when the temperature increases; accordingly, from Eq. 4, the noise performance will be degraded[3].

In the above derivation, it is assumed that the gate-

source biasing voltage V_{gs} is constant, but for a conventional biasing circuit, V_{gs} does vary with the temperature. In other words, the current in the biasing branch varies with the temperature and has a negative value, which further degrades the performance of the low-noise amplifier[3]. The mixer can also be analyzed in the same way.

To solve the above problem, there are two solutions. The first method uses a biasing current with a positive temperature coefficient[3]. The second solution is to increase the supply voltage to increase the g_m value. In this paper, the second method is utilized.

Ⅲ. Top Level Architecture

Fig. 3 shows a detailed description of a CMOS RF front-end with the temperature compensation scheme. There are three major blocks: the LNA, the mixer, and the variable voltage supply.

3-1 Variable Voltage Supply

In CMOS technology, substrate vertical p-n-p bipolar junction transistors implement the p-n junctions. In the detailed circuit of Fig. 3, the voltages at the nodes are kept equal by the op amp V_a=V_b. As the currents in MP1 and MP2 are equal, IMP1=IMP2=I1, and the voltage drop on R1 is $(kT/q)\ln M$, where M is the ratio of the emitter areas. The current I1 is then

$$I_1 = \frac{1}{R1}\frac{kT}{q}\ln M \tag{8}$$

Therefore, the voltage Vbg is

$$Vbg = n\frac{R2}{R1}\frac{kT}{q}\ln M + V_{BE3} \tag{9}$$

Here, the first contribution is PTAT. It has a positive temperature coefficient of 0.086 mV/℃ while the second decreases with the temperature coefficient of −2 mV/℃. By choosing the appropriate n, R1, R2 and M values, a Vbg value with very low temperature sensitivity can be obtained[6].

The V_c node is VBE3. This node changes according to the temperature. The differential op amp change V_c to the proper value (V_e) using R9 and the single op amp add V_d and V_e as well as amplify using the ratio of R. In this case, V_d has very low temperature sensitivity due to the state of Vbg. In order to produce variable voltages up to 2.2 V, a single op amp is supplied the power from the Vsource and add V_d to V_e. V_f and V_g kept equal by M1, M2, M3, M4 and M5. M5 forms the current path, and V_g supplies the voltage to the LNA and the mixer. Fig. 4 shows the voltages for all nodes.

3-2 Low Noise Amplifier

The LNA topology (Fig. 5) uses a common-source amplifier tuned to 2.4 GHz with cascode transistors to maximize reverse isolation and an inductor degeneration scheme that uses a bond wire to achieve real-part impedance up to 50 ohm[7]. The gain is programmable between 25 dB and 11 dB. The NF is 1.5 dB in the high-gain mode.

3-3 Mixer

Given that MOS transistors have much higher IIP3 values than bipolar transistors, it is possible to integrate "linear" mixers. Therefore, more gain can be assigned to the LNA, which relaxes the noise specs of the mixers.

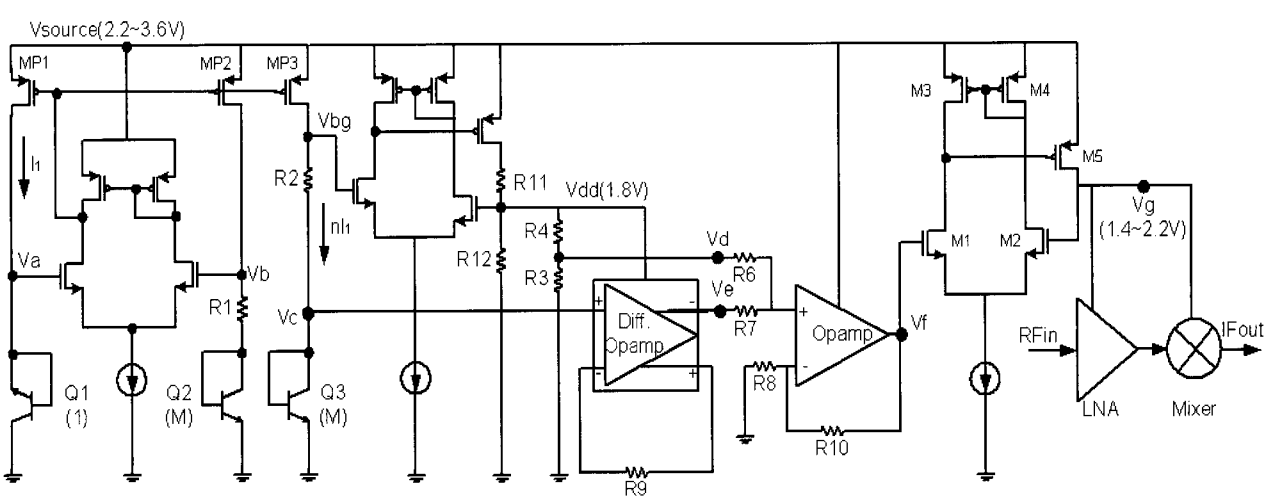


Fig. 3. A detailed circuit description of the CMOS RF front-end circuit with the temperature compensation scheme.

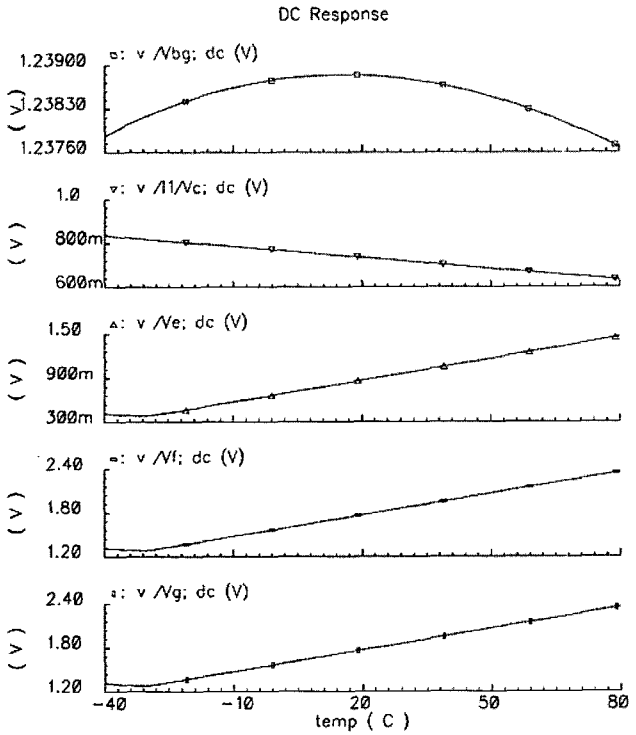


Fig. 4. Variation of the voltage with the temperature.

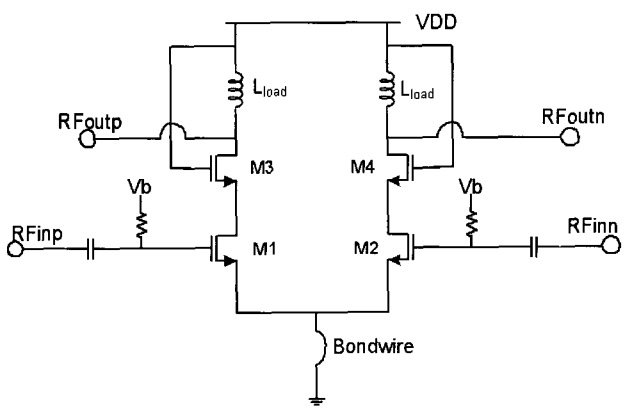


Fig. 5. LNA topology.

In the circuit topology of Fig. 6, the down-conversion mixer employs a Gilbert cell mixer topology[2]. The quadrature architecture reduced LO leakage and LO self-mixing. The gain is programmable between 9.5 dB and −10 dB.

Ⅳ. Experimental Results

A photomicrograph of a CMOS RF front-end is shown in Fig. 8. The results described in this paper were obtained from a COB(Chip On Board). The measurement results of the front-end are shown in Fig. 7. The simulation and measurement results show that the

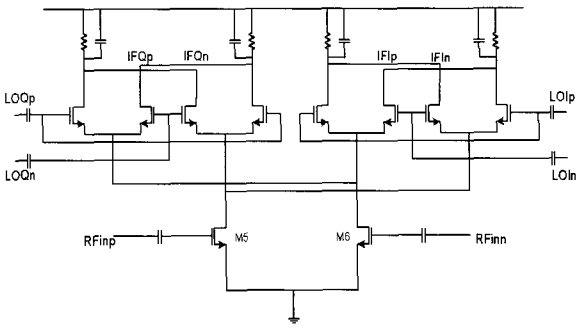
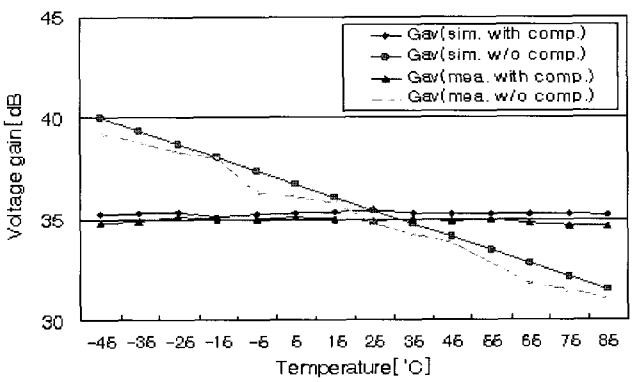
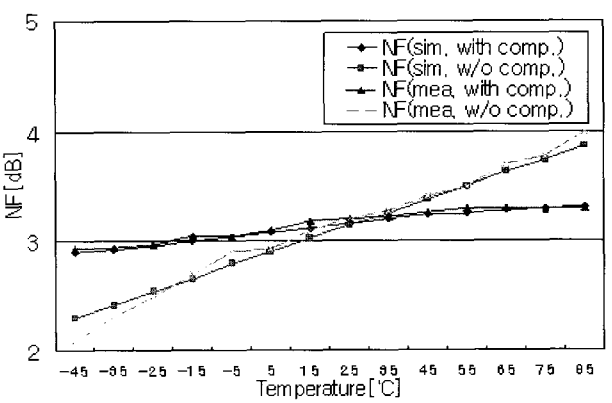


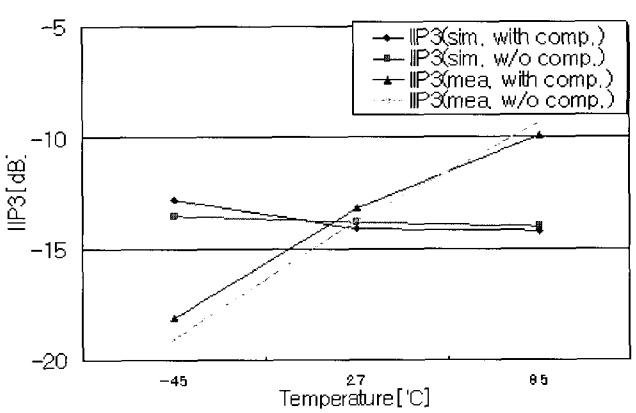
Fig. 6. Down conversion mixer topology.



(a) Voltage gain results



(b) Noise figure results



(c) IIP3 results

Fig. 7. Simulation and measurement results.

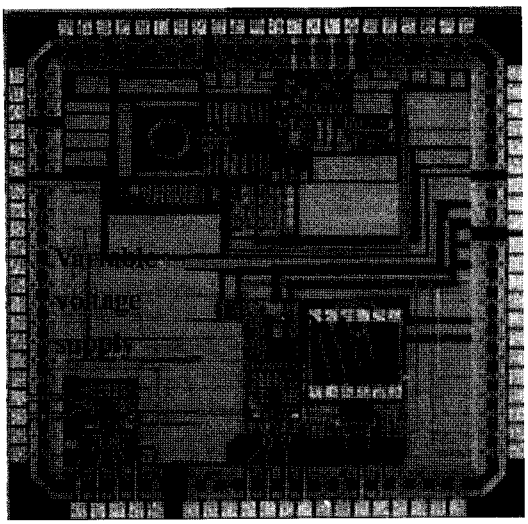


Fig. 8. Chip micrograph.

Table 1. Performance comparison of CMOS front-end

Ref.	Freq [GHz]	Process [um]	Gain variation [dB]	NF variation [dB]	IIP3 variation [dB]
[3]	2.4	0.35	0.4	0.1	-
This work	2.4	0.18	0.2	0.25	1.5

front-end (LNA, Mixer) can achieve a 35.3 dB voltage gain and a 3.1 dB noise figure while consuming 2.16 mW of power at 27 ℃. The voltage gain, noise figure and third-order intercept point(IIP3) variations over −45 ℃ to 85 ℃ are less than 0.2 dB, 0.25 dB and 1.5 dB, respectively. This front-end has achieved comparable performance to the other CMOS front-end using temperature compensation as shown in Table 1.

Ⅴ. Conclusion

A temperature-compensated RF front-end is developed in this paper. It is implemented in 0.18 um CMOS technology with a nearly flat voltage gain, noise figure as the temperature ranges from −45 ℃ to 85 ℃ and the power supply varies from 2.2 V to 3.6 V. Power consumption less than 2.16 mW is suitable for low-power applications. A more robust system for severe temperature environments can be created if this is applied to a transceiver.

References

[1] S. E. Nordquist, J. W. Haslett, and F. N. Trofimenkoff, "High temperature leakage current suppression in CMOS integrated circuits", *Electronics Lett.*, vol. 25, no. 17, pp. 1113-1135, 1989.

[2] Behzad Razavi, *RF Microelectronics: Prentice Hall Communications Engineering and Emerging Technologies Series*, 1998.

[3] Yue Wu, Chunlei Shi, "Temperature compensation desing for A 2.4 GHz CMOS low noise amplifier", *IEEE International Symposium on Circuits and Systems*, pp. 323-326, 2000.

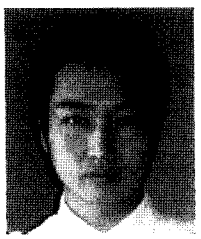
[4] Y. P. Tsividis, *Operation and Modeling of the MOS Transistor*. New York: McGraw-Hill, 1987.

[5] T. Manku. "Microwave CMOS devices and circuit", in *Proc. IEEE 1998 Custom Integrated Circuit Conf.*, pp. 59-66, 1998.

[6] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuit*, Cambridge, 1998.

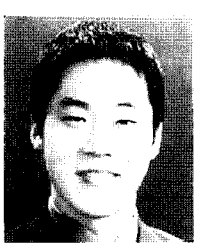
[7] P. Leroux, J. Janssens, and M. Steyaert, "A 0.25 _m CMOS LNA with local impedance matching", Dept. Elect. Eng., Master's thesis, K.U. Leuven, Leuven, Belgium, 1999.

Yong-Il Kwon



received the M.S. degree in electronics engineering from Ajou University, Suwon, Korea, in 2006, He is currently working toward the Ph.D. degree at the Microwave application Lab of Ajou University. His thesis is on the low power 2.4 GHz CMOS RF receiver for LR-WPAN(IEEE 802.15.4) applications. He joined Samsung electro-mechanics, R&D institute in 2000 where he has been engaged in the design and testing of both CMOS RFIC and RF system. He was also an analog design lead for CDMA modem and PLC(Power Line Communication) modem products. His research interests include microwave circuit design, telecommunications, antenna systems, high-frequency analog integrated circuits and continuous time sigma delta bandpass ADC.

Sangwoon Jung



received the B.S. degree in information communication engineering from Seokyeong University, Seoul, Korea, in 2006. He is currently working toward the M.S. degree in the Department of Electronics Engineering at Ajou University, Suwon, Korea. His research interests include in the microwave passive component design, SI/EMC and RFIC.

Hai-Young Lee

received the B.S. degree in electronics engineering from Ajou University, Suwon, Korea, in 1980, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Seoul, Korea, in 1982, and the Ph.D. degree in electrical engineering from The University of Texas at Austin, in 1989. From 1982 to 1986, he was with the Ministry of National Defense, Seoul, Korea, as a senior research engineer in the fields of electromagnetic compatibility and wave propagation. In 1998, he was a visiting professor at the University of California at Los Angeles. From 1990 to 1992, he was in charge of the Advanced Research Division I(Compound Semiconductor Devices Division) at the Goldstar Central Research Laboratory(currently the LG Electronics Institute of Technology), Seoul, Korea. Since 1992, he has been with the Department of Electronics Engineering, Ajou University, Suwon, Korea, as a Professor. He serves for the president of the User Council at Korea Advanced Nano Fab Center, Suwon, Korea. His current research interest lies in the fields of RFIC design and testing, system-on-a-package(SOP), and high-speed interconnections and EMI/EMC for digital applications.