A Parallel Coupled QVCO and Differential Injection-Locked Frequency Divider in 0.13 μm CMOS

Bong-Hyuk Park · Kwang-Chun Lee

Abstract

A fully integrated parallel-coupled 6-GHz quadrature voltage-controlled oscillator (QVCO) has been designed. The symmetrical parallel-coupled quadrature VCO is implemented using 0.13-μm CMOS process. The measured phase noise is -101.05 dBc/Hz at an offset frequency of 1 MHz. The tuning range of 710 MHz is achieved with a control voltage ranging from 0.3 to 1.4 V. The average output phase error is about 1.26° including cables and connectors. The QVCO dissipates 10 mA including buffer from the 1.5 V supply voltage. The output characteristic of the differential injection-locked frequency divider (DILFD), which has similar topology to the QVCO, is presented.

Key words : QVCO, CMOS, Phase Noise, Phase Error, DILFD.

I . Introduction

An accurate quadrature signal is a prerequisite for the implementation of an image-rejection transceiver[1]. There are several methods to generate a quadrature signal in a local oscillator. The most popular method is to let the VCO work at double the desired frequency, and then to obtain quadrature signals at the desired frequency via frequency division[2]. The frequency division approach has a beneficial effect on avoiding a pulling effect of the VCO due to the strong signal of the same frequency inthe power amplifier. The second method of obtaining quadrature signals is through the use of a polyphase filter, usually realized as an RC polyphase filter[3]. A third way of implementing quadrature signals is the adoption of a VCO design capable of directly delivering such signals, namely QVCO. In the past, many topologies of QVCO have been published; two cross-coupled VCOs forced to run in quadrature by using two additional pairs of parallel-coupling transistors[4], a series-type QVCO that is implemented using the symmetrical coupling method[5]. Since the series QVCO is associated with voltage headroom, it is not an appropriate architecture for low-voltage operation. However, the phase noise characteristic of series QVCO is better than parallel QVCO. The parallel QVCO is usually applied for reducing IQ mismatch and low-voltage applications.

In this paper, a symmetrical parallel-coupled QVCO topology for minimizing phase error and differential injection-locked frequency divider are presented.

II . Circuit Description

Fig. 1 shows the multi-band signal generator architecture. The 6-GHz band QVCO makes the in-phase and quadrature-phase signal, and then these signals are mixed with a quadrature single-side band (SSB) mixer. In order to not feed through the local signal in the SSB mixer, the exact quadrature signal generation is important. QVCO has a better signal quality than divide-by-two and polyphase filter methods in generating quadrature signal. Therefore, QVCO is applied in this multi-band generator system.

The circuit of the symmetrical parallel-coupled QVCO is shown in Fig. 2. Usually, the parallel QVCO delivers four quadrature signals exhibiting low phase and amplitude errors, but it has not been used extensively because of the rather poor phase noise performance. Therefore, the PMOS and NMOS symmetrical-type parallel QVCO is adopted to reduce phase noise in this paper. The coupling transistors M3, M4, M9, and M10 are placed in parallel with the switch transistors M1, M2, M7, and M8. The outputs of each VCO are connected to coupling transistors.

The coupling factor α is defined as the ratio of the width of the coupling transistor (W_{CPL}) to the width of the switch transistor (W_{SW})[6].

$$\alpha = \frac{W_{CPL}}{W_{SW}} \tag{1}$$

where $\alpha = 1$ is chosen in order to improve the phase/amplitude error performance.

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Mobile RF Research Team, Electronics and Telecommunications Research Institute, Daejeon, Korea.

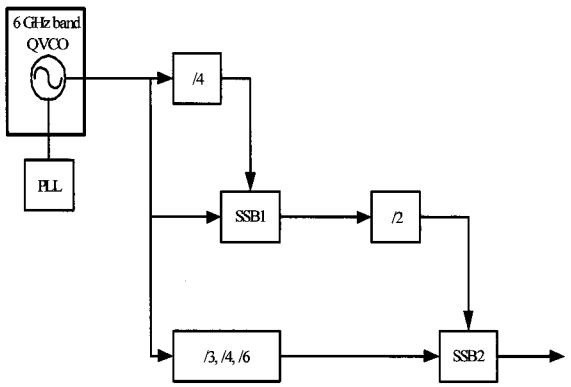

Fig. 1. Multi-band signal generator architecture.

Fig. 3 shows the schematic of the voltage-controlled DILFD used in the high-frequency divider. The differential incident signal(the VCO output) is injected into the gates of M13 and M14. The output signal is fed back to the gates of M1, M2, M7, and M8 and is summed with the incident signal across the gates and sources of M1, M2, M7, and M8. This circuit has a natural tendency for divide-by-two operation when the incident signal is effectively injected into the gates of M13 and M14.

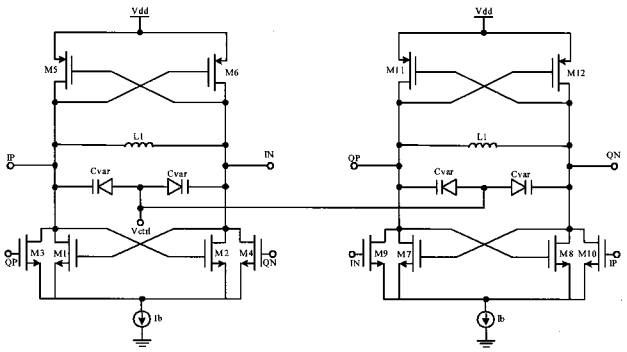

Fig. 2. Symmetrical parallel-coupled QVCO.

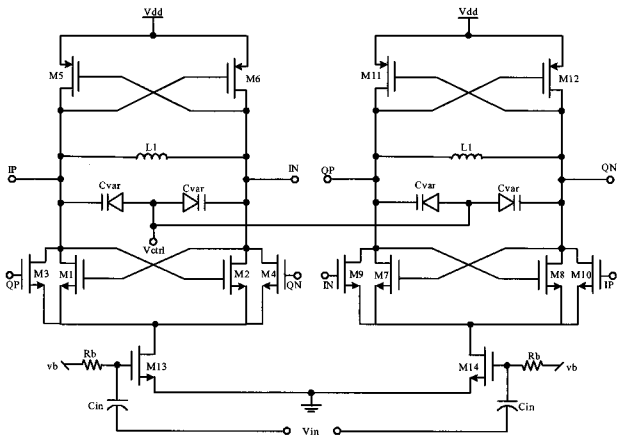

Fig. 3. Differential injection-locked frequency divider.

Ⅲ. Measurement Results

Fig. 4 shows the photograph of the symmetrical parallel-coupled QVCO. The chip size is 980×580 μm^2 including the pads. The measurements were done with a 1.5-V power supply and a current consumption of 6.0 mA in the core circuit. Fig. 5 shows the output spectrum near the center frequency of the QVCO. The harmonic characteristic of the QVCO is given in Fig. 6. It shows that the harmonic suppression of the QVCO is larger than 24 dBc. Fig. 7 shows the measured time-domain output waveforms of the QVCO output buffers. The average output phase error is about 1.26°, introduced partly by cables and connectors.

As shown in Fig. 8, the measured phase noise is −101.05 dBc/Hz at 1-MHz offset. The normalized phase noise has been defined as a figure-of-merit(FOM)[7].

The FOM of the QVCO is about −167.4 dBc/Hz.

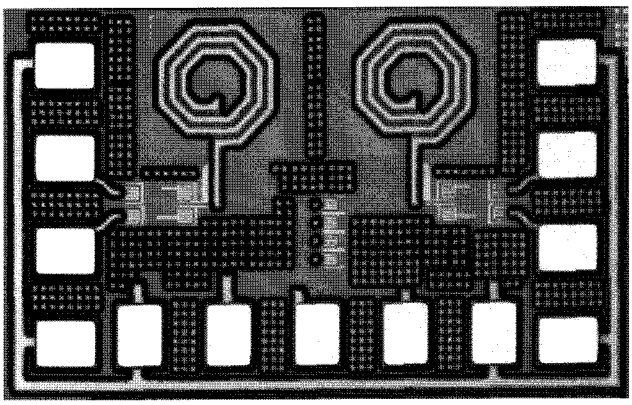

Fig. 4. Chip photograph of QVCO.

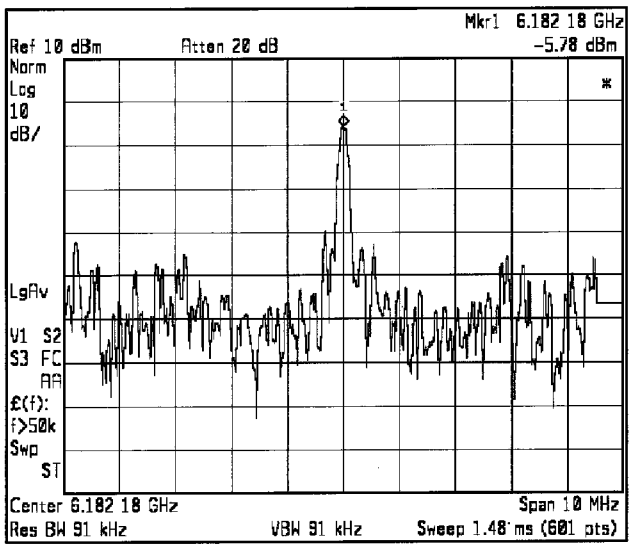

Fig. 5. Output spectrum at the center frequency of the QVCO.

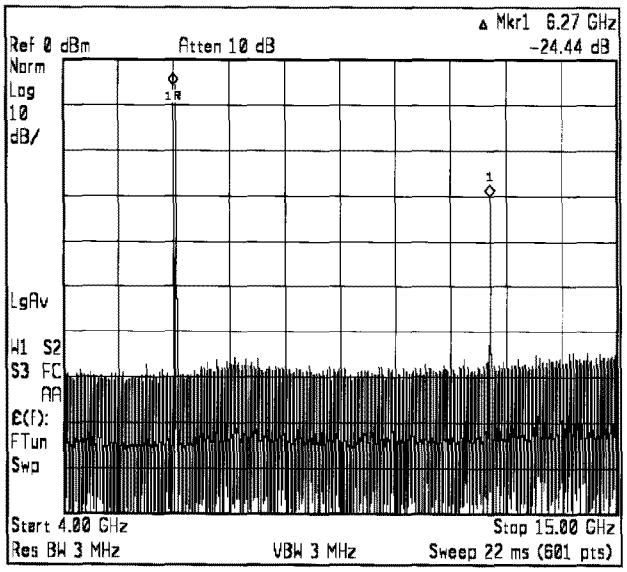

Fig. 6. Harmonic characteristic of the QVCO.

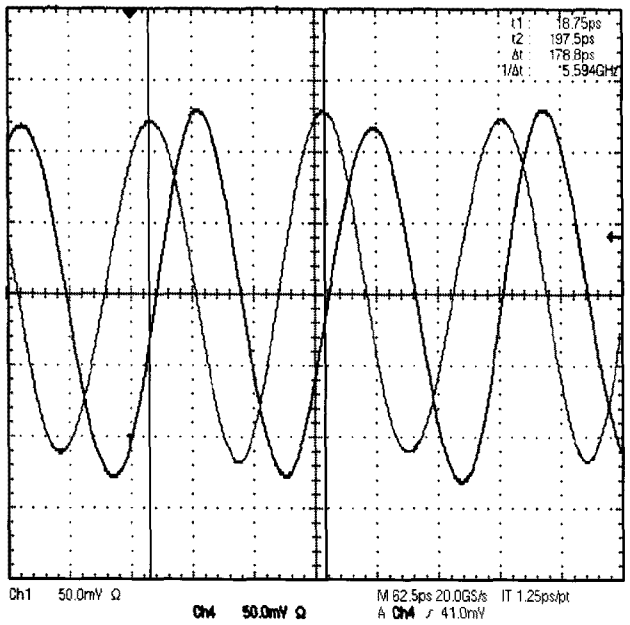

Fig. 7. Measured output waveforms of the I and Q channels.

$$FOM = 10\log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \frac{1}{L\{\Delta\omega\}P}\right] \quad (2)$$

A comparison of the CMOS LC VCO based on the FOM is summarized in Table 1.

Fig. 9 shows the micrograph of the differential injection-locked frequency divider. The chip size is 1,200× 720 μm^2 including the pads. The layout was made as symmetrical and compact as possible to ensure differential operation and reduce parasitic inductance or capacitance. The experiments were done with a 1.2-V power supply and a current consumption of 4.3 mA in the core circuit.

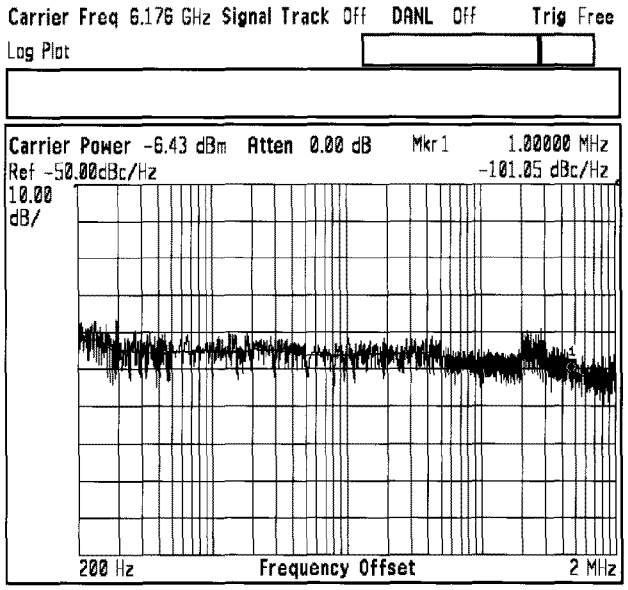

Fig. 8. Measured phase noise of the QVCO.

Table 1. Performance comparison.

Ref	Fc (GHz)	VDD (V)	Itail (mA)	Phase noise (1-MHz offset)	FOM (dBc/Hz)
[8]	7.65	1.8	8.0	−110	−176.6
[9]	8.0	1.8	8.3	− 94.7	−161.4
This work	6.2	1.5	6.0	−101.05	−167.4

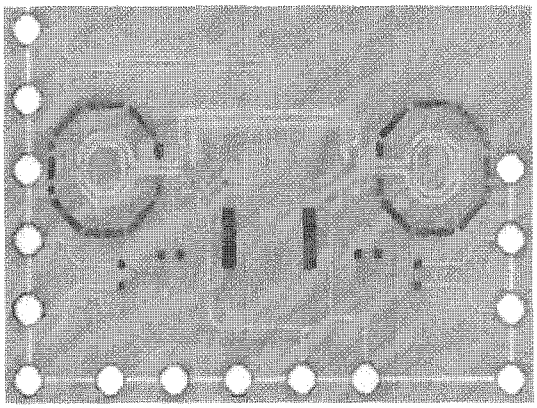

Fig. 9. Chip micrograph of differential ILFD.

The 16-GHz band incident signal is injected into the input node, and the differential ILFD's output is measured with a spectrum analyzer while tuning control voltage. Fig. 10 shows the output spectrum at the center frequency of the DILFD.

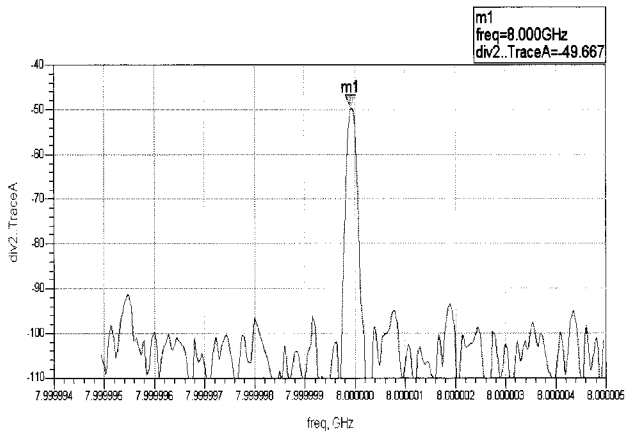

Fig. 10. Output spectrum at the center frequency of the DILFD.

Ⅳ. Conclusion

In this paper, we have presented a fully integrated symmetrical parallel-coupled LC QVCO and differential injection-locked frequency divider. The QVCO core consumes 6.0 mA from a 1.5-V supply and achieves −101.05 dBc/Hz phase noise at 1-MHz offset from the 6.2-GHz carrier. The figure of merit is −167.4 dBc/Hz.

The differential ILFD core dissipates 4.3 mA from 1.2-V power supply and shows the 16-GHz band-dividing characteristic. These circuits were fabricated with 0.13-μm CMOS technology.

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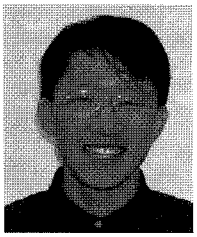
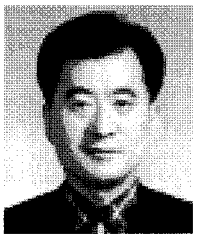
Bong-Hyuk Park



received the B.S. degree in electrical engineering from Kyungpook National University, Korea, in 1996, and the M.S. degree in mechatronics from Gwangju Institute Science and Technology(GIST), Gwangju, Korea, in 1998, respectively. He received the Ph.D. degree in electrical engineering from Korea Advanced Institute of Science and Technology(KAIST), Korea, in 2010. From 1998 to 1999, he worked as an RF Application Engineer at Ansoft. Since 1999, he has been with Electronics and Telecommunications Research Institute(ETRI). His main research interests include UWB RF transceiver front-end circuit design, frequency synthesizers and system-level integration of transceivers.

Kwang-Chun Lee



received the B.S./M.S. degree in electronic engineering from Chungang University, Korea, in 1986/1988 respectively. Since 1988, he has been with Electronics and Telecommunications Research Institute(ETRI). His main research interests include high efficiency power amplifier and RF technologies for mobile communication system design.