JOURNAL OF ELECTROMAGNETIC ENGINEERING AND SCIENCE, VOL. 13, NO. 2, 127～133, JUN. 2013

http://dx.doi.org/10.5515/JKIEES.2013.13.2.127
ISSN 2234-8395 (Online) · ISSN 2234-8409 (Print)

Scaling Rules for Multi-Finger Structures of 0.1-μm Metamorphic High-Electron-Mobility Transistors

Pil-Seok Ko · Hyung-Moo Park*

Abstract

We examined the scaling effects of a number of gate_fingers (N) and gate_widths (w) on the high-frequency characteristics of 0.1-μm metamorphic high-electron-mobility transistors. Functional relationships of the extracted small-signal parameters with total gate widths (w_t) of different N were proposed. The cut-off frequency (f_T) showed an almost independent relationship with w_t; however, the maximum frequency of oscillation (f_{max}) exhibited a strong functional relationship of gate-resistance (R_g) influenced by both N and w_t. A greater w_t produced a higher f_{max}; but, to maximize f_{max} at a given w_t, to increase N was more efficient than to increase the single gate_width.

Key Words: Scaling Rule, HEMT, Small-Signal Parameters, Gate Width.

Ⅰ. Introduction

High-electron-mobility transistors (HEMTs) have been highlighted as essential high-frequency devices for various state-of-the-art microwave or millimeter-wave application systems, such as satellite communication, electronic warfare, radiometry, base stations, and smart weapons [1-3]. These systems require not only excellent radio frequency (RF) characteristics but also high-power performances for their specific applications [4]. The enhancement of power characteristics can be achieved by improving the current level or breakdown voltage of the HEMTs. A variety of methods have been used to increase the power performance of HEMTs these include the GaN/AlGaN material system [5, 6], the gate-field-plate technique [7, 8], and the adoption of composite channel systems [9, 10]. Most of these methods have focused on the enhancement of transistor power by increasing the breakdown voltage. These technologies, however, have some drawbacks, such as high cost and difficulty in material growth of the composite channel HEMTs, poor RF characteristics of the GaN HEMTs, and low electron mobility and large increase in the parasitic capacitances of the gate-field-plated HEMTs. As a consequence, in many application achieving a large current level by simply increasing the transistor gate_width (w) has been one of the most economic and practical methods in terms of circuit design and device fabrication.

A very long gate width or multi-finger gates are effective, but an increase in w gives rise to a large gate resistance (R_g), thereby causing degradation of noise characteristics [11] and the maximum frequency of oscillation (f_{max}) [12]. Therefore, it preferable to achieve a long effective gate width with no significant increase or even reduction in R_g. The use of a wide-head T-gate was reported [11] as an exemplary method for suppressing R_g; however, this technique has a limit in expanding the gate head because high source-to-drain channel resistance is unavoidable under increased source-drain spacing for accommodating a wide gate-head dimension; consequently, the structural instability of the T-gate increases in this structure. Even though studies [13-15] have documented the critical role of R_g in the high-frequency characteristics of HEMTs based on a small-signal-equivalent circuit model, there has been minimal investigation in reducing R_g in HEMTs with long gate_widths or multi-finger gates. In this study, we investigated the multi-finger structures of the HEMTs affecting R_g and high-frequency characteristics. Because R_g is strongly influenced by a number of gate_fingers (N) and gate_widths (w) of the device structure, we examined the effects of all these parameters on R_g and the device characteristics by using various combinations of struc-

Manuscript received April 23, 2013 ; Revised May 28, 2013 ; Accepted May 30, 2013. (ID No. 20130423-015J)
Division of Electronics and Electrical Engineering, Dongguk University, Seoul, Korea.
*Corresponding Author : Hyung-Moo Park (e-mail : parkhm@dongguk.edu)

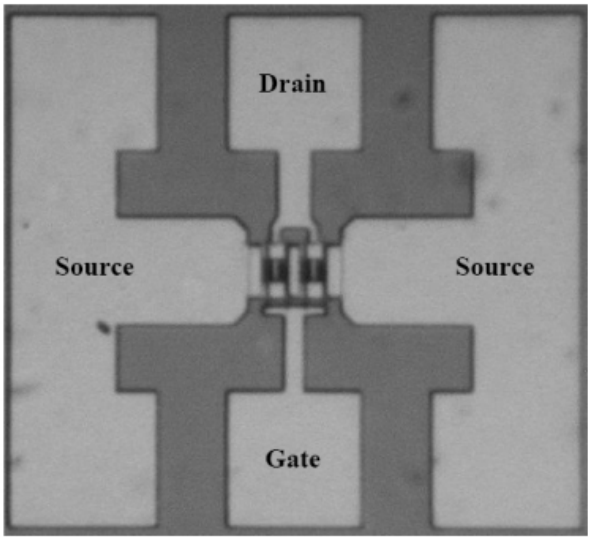


Fig. 1. Micrograph of the fabricated chip with the four-finger metamorphic high-electron-mobility transistors.

tural parameters for the 0.1-μm depletion-mode InGaAs/InAlAs metamorphic HEMT (MHEMT). To investigate the effects of N and w, 12 different gate peripheries were fabricated with various gate fingers (2, 4, and 6) and gate widths (25, 40, 50, and 70 μm). Except for the variations in N and w, we maintained the same epitaxial structure, gate length of 0.1-μm, and source-drain spacing of 2-μm for all fabricated devices, as described in the next section.

The MHEMT micrograph of the HEMT with four fingers is shown in Fig. 1.

Ⅱ. Device Fabrication

As shown in Fig. 2, the MHEMT epitaxial structure was grown by molecular beam epitaxy on a semi-insulating GaAs substrate. The structures consisted of the following layers from the bottom: a 1000-nm $In_xAl_{1-x}As$ linearly graded buffer layer with an indium mole fraction, x, linearly graded from 0 to 0.5; a 300-nm undoped $In_{0.52}Al_{0.48}As$ buffer layer; a silicon delta-doped plane (1.3×10^{12}/cm^2), a 4-nm undoped $In_{0.52}Al_{0.48}As$ spacer layer; a 23-nm undoped $In_{0.53}Ga_{0.47}As$ channel layer; a 3-nm undoped $In_{0.52}Al_{0.48}As$ spacer layer; a silicon delta-doped plane (4.5×10^{12}/cm^2); a 15-nm undoped $In_{0.52}Al_{0.48}As$ Schottky barrier layer; and a 15-nm n-type $In_{0.53}Ga_{0.47}As$ cap layer (6×10^{18}/cm^3). The grown epitaxial layer showed a two-dimensional electron carrier density (n_s) of about 3.5×10^{12}/cm^2 and a Hall mobility of about 9,700 cm^2/Vsec at room temperature.

To fabricate the MHEMTs, we first isolated active areas by using mesa etching with an etchant of phosphoric acid/H_2O_2/H_2O (1:1:60) to reduce the thickness to

n^+ Cap Layer (6×10^{18}/cm^3)	$In_{0.53}Ga_{0.47}As$	15 nm
i - Schottky Barrier Layer	$In_{0.52}Al_{0.48}As$	15 nm
Si delta doping (4.5×10^{12}/cm^2)		
i - Spacer Layer	$In_{0.52}Al_{0.48}As$	3 nm
i - Channel Layer	$In_{0.53}Ga_{0.47}As$	23 nm
i - Spacer Layer	$In_{0.52}Al_{0.48}As$	4 nm
Si delta doping (1.3×10^{12}/cm^2)		
i - Buffer Layer	$In_{0.52}Al_{0.48}As$	300 nm
i - Graded buffer Layer	$In_xAl_{1-x}As$ (X = 0 ~ 0.5)	1000 nm
Semi - insulating GaAs Substrate		

Fig. 2. Epitaxial structure of the metamorphic high-electron-mobility transistor.

200-nm. AuGe/Ni/Au (140/30/160 nm) ohmic metallization showed a specific contact resistance of about 5×10^{-7} Ω-cm^2 after rapid thermal annealing at 320℃ for 60 seconds in a vacuum. An electron beam lithography system (EBPG-4HR, Leica Microsystems Ltd., Buffalo Grove, IL, USA) was used to perform 0.1-μm T-shaped gate patterning upon completion gate_recess, gate metallization was performed by evaporating Ti/Au (50/400 nm) followed by metal lift-off. The MHEMTs were passivated with the Si_3N_4 films (80 nm). Finally, a Ti/Au (30/700 nm) air-bridge interconnection was made to connect the source pad.

Ⅲ. Analysis of Device Scaling

The DC characteristics of each MHEMT were measured in an HP 4156 DC parameter analyzer. Drain current (I_{ds}) versus gate voltage (V_{gs}) and transfer characteristics of the MHEMTs (at a drain voltage [V_{ds}] of 1.2 V) were measured at various N and w values. With the total gate width (w_t), the saturation drain current (I_{dss}) and maximum transconductance ($g_{m,max}$) were linearly increased at constant slopes of about 0.58 mA/μm and 0.57 mS/μm, respectively, as shown in Fig. 3. The w_t is hereafter defined as "total gate width" and given by the product of N and w. The scaling rules for these parameters are then simply expressed as:

$$\frac{I_{dss}^1}{I_{dss}^2}=\frac{g_{m,\max}^1}{g_{m,\max}^2}=\frac{w_t^1}{w_t^2} \quad (1)$$

High-frequency characteristics of the fabricated MHEMTs were measured in the frequency range of 0.5 to 50 GHz using an HP8510C network parameter analyzer (Agilent Technologies, Palo Alto, CA, USA). Cut-off frequency (f_T) and f_{max} were determined by extrapolating the h_{21} and U gain curves, respectively, at a slope of 6 dB/octave. The DC and RF data were measured from each gate type of the MHEMTs at six different dies on

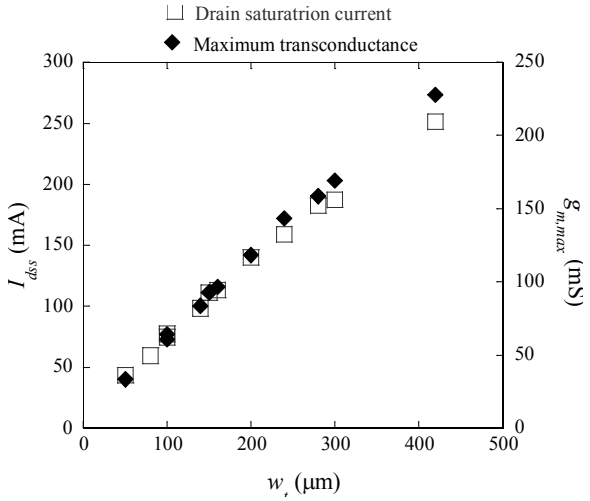
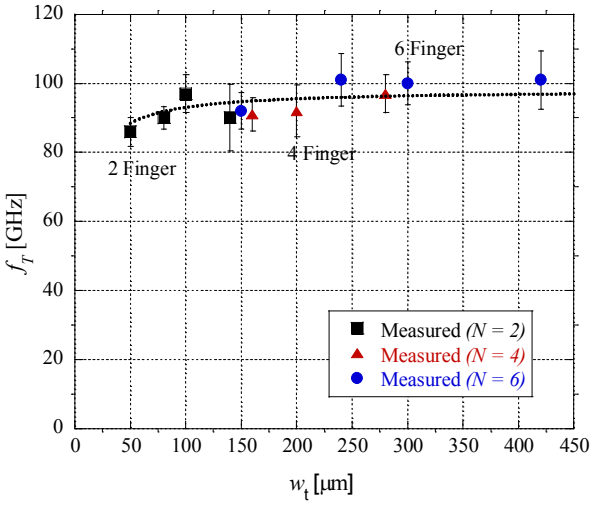
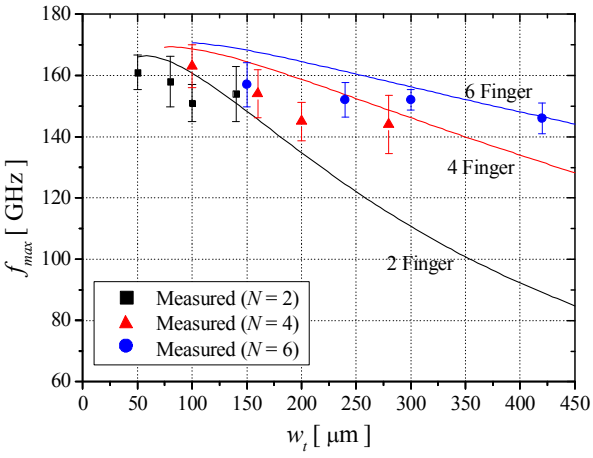


Fig. 3. I_{dss} and g_m versus w_t of the metamorphic high-electron-mobility transistors at various N.



(a)



(b)

Fig. 4. Average f_T and f_{max} as functions of the w_t measured from the metamorphic high-electron-mobility transistors of twelve different gate types and six different dies (calculation, solid line; measurement, symbols).

Table 1. Fitting equations of the small-signal parameters

Parameter	Fitting equation
C_{gs}	$C_{gs} = 0.00089 w_t$
C_{gd}	$C_{gd} = 0.0049 + 0.000087 w_t$
G_{ds}	$G_{ds} = 0.0355 w_t$
$g_{m,int}$	$g_{m,\mathrm{int}} = 0.614 w_t$
R_i	$R_i = 1{,}580 / w_t$
R_s	$R_s = 190 / w_t$

a 2.5×2.5 cm^2 specimen. The average f_T and f_{max} from the MHEMTs with 12 different gate types measured from six different dies were plotted respectively in Fig. 4 with their standard deviations (1 σ). The f_T increased slightly in a small w_t region and was saturated to a frequency of about 100 GHz; on the other hand, the f_{max} decreased continuously with the w_t in our whole experimental range of w_t, and the reduction ratio was a function of N.

To examine the effects of N and w_t on the small-signal parameters directly affecting f_T and f_{max}, all the parameters shown in Eqs. (2) and (3) [16, 17] were extracted from the fabricated MHEMTs by the Dambrine method [18] and curve-fitted to simple functions of w_t. As shown in Table 1, gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), drain conductance (G_{ds}), and intrinsic transconductance ($g_{m,int}$) were proportional to w_t.

However, intrinsic resistance (R_i) and source resistance (R_s) were inversely proportional to w_t. All these parameters were functions of w_t. But were not functions of N; however, one exception was R_g, which was a function of both w_t and N.

$$f_T = \frac{g_{m,\mathrm{int}}}{2\pi\left(C_{gs}+C_{gd}\right)\left(1+G_{ds}\cdot R_s\right)+C_{gd}g_{m,\mathrm{int}}R_s} \approx \frac{g_{m,\mathrm{int}}}{2\pi C_{gs}} \tag{2}$$

$$f_{\max} = \frac{f_T}{\sqrt{4G_{ds}\left(R_g+R_s+R_i\right)+4g_{m,\mathrm{int}}R_g\dfrac{C_{gd}}{C_{gs}+C_{gd}}}} \tag{3}$$

The relationships of the fitted parameters with w_t can be explained as follows. C_{gs} is a function of C_{gso} which is gate-to-source capacitance per unit gate width, and therefore is expressed as

$$C_{gs} = C_{gso} \times N \cdot W = C_{gso} \times w_t \tag{4}$$

where C_{gso} is about 0.00089 pF/μm in our case. In the case of the C_{gd}, y-axis intercepts should also be considered. A non-zero C_{gd} at zero w_t can be formed between

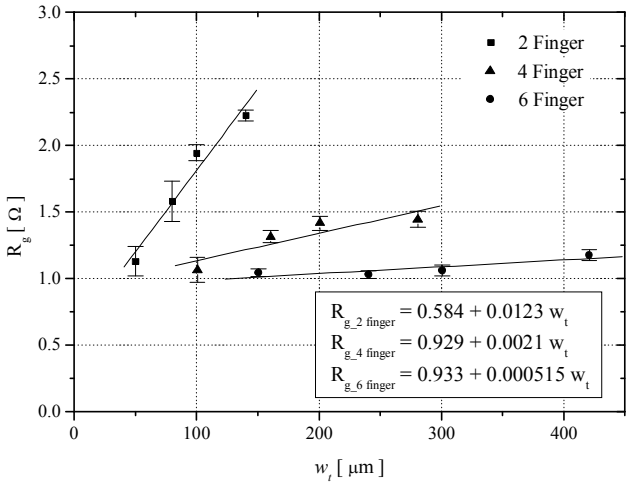


Fig. 5. Extracted R_g as functions of w_t (fitting, solid line; measurement, symbols).

the gate bus line and drain pad and this parasitic capacitance, in fact, has been observed in earlier studies [13, 19, 20]. In our case, the y-axis intercept of C_{gd} was about 0.0049 pF, and the proportionality constant was about 0.000087 pF/μm. The linear relationship of G_{ds} with w_t can be understood such that the total source-drain conductance is given by (dI_{ds}/dV_{ds} per unit gate width)×w_t, and the corresponding proportionality constant was about 0.0355 mS/μm in our case. R_s and R_i were inversely proportional to w_t and curve-fitted in the same way with the proportionality constants of about 190 and about 1,580 Ω · μm, respectively. The linear increase of $g_{m,int}$ with w_t can be explained by the linear scaling rule of $g_{m,ext}$ with w_t, as shown in Eq. (1); the proportionality constant was about 0.614 mS/μm.

$$R_g = R_o + \rho_G \frac{W}{3AN} = R_o + \rho_G \frac{w_t}{3AN^2} \tag{5}$$

R_g is a function of both N and w_t, as shown in Fig. 5, and can be expressed as Eq. (5) where ρ_G is the resistivity of the gate metal, and A is the cross-sectional area of the gate. R_o is the y-axis intercept obtained by linear curve fitting. This relationship can be obtained by assuming the gradual (linear) reduction in gate current (I_g) density as the open end is approached, as illustrated in Fig. 6, and an essentially uniform displacement current fed from the bottom of the gate to the channel region of the HEMTs [21]. In the open-ended gate structure shown in Fig. 6, I_g and the infinitesimal change of V_{gs} (δV_{gs}) over δx are given by Eqs. (6) and (7),

$$I_g(x) = I_{go}\left(1 - \frac{x}{w}\right) \tag{6}$$

$$\delta V_{gs}(x) = -I_g(x) \cdot \delta R(x) = -I_{go}\left(1 - \frac{x}{w}\right) \cdot \rho_G \left(\frac{\delta x}{Lh}\right) \tag{7}$$

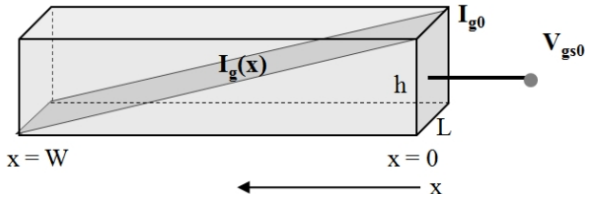


Fig. 6. Distribution of gate current in the gate-width direction.

where L and h are gate-length and gate-height, respectively. The minus sign in Eq. (7) indicates that gate voltage decreases with increasing x. At x=0, V_{gs} is equal to V_{gs0}, gate terminal voltage. Gate voltage V_{gs} (x) is obtained by integrating Eq. (7) with the boundary condition at x=0.

$$V_{gs}(x) = -\left(\frac{I_{go} \cdot \rho_G}{Lh}\right)\left(x - \frac{x^2}{2w}\right) + V_{gs0} \tag{8}$$

The average gate voltage is equal to the integral of V_{gs} (x) from x=0 to W and then divided by W. After carrying out the definition, we find the average value to be

$$\overline{V_{gs}} = -\frac{1}{3}\frac{w}{Lh} I_{go} \cdot \rho_G + V_{gs0} \tag{9}$$

The average intrinsic gate resistance inside the gate electrode region from x=0 to w is then given by:

$$\overline{R_g} = \frac{V_{gs0} - \overline{V_{gs}}}{I_{go}} = \frac{1}{3}\frac{w}{Lh} \cdot \rho_G = \frac{1}{3}\frac{w}{A} \cdot \rho_G \tag{10}$$

Investigations have focused on R_o, R_g when w approaches zero [21, 22]; however, the model for R_o, is still not fully understood. In our case, the y-axis intercepts of the MHEMTs (N=2, 4, and 6) range from about 0.6 to 0.9 Ω, with the corresponding proportionality constants of about 0.0123, 0.0021, and 0.000515 Ω/μm, respectively, as shown in Fig. 4. Therefore, the scaling rules of the small-signal parameters can be summarized as follows:

$$\frac{C_{gd}^1}{C_{gd}^2} \approx \frac{C_{gs}^1}{C_{gs}^2} = \frac{G_{ds}^1}{G_{ds}^2} = \frac{g_{m,\mathrm{int}}^1}{g_{m,\mathrm{int}}^2} = \frac{w_t^1}{w_t^2} \tag{11}$$

$$\frac{R_i^1}{R_i^2} = \frac{R_s^1}{R_s^2} = \frac{w_t^2}{w_t^1} \tag{12}$$

$$R_g \propto w_t \text{ and } \frac{1}{N^2} \tag{13}$$

f_T and f_{max} can be calculated by substituting each small-signal parameter of Eqs. (2) and (3) with the curve-fitting equations in Table 1. The calculated results are plotted in Fig. 4 with measurements at each N and

w_t. Good agreement was obtained from the calculated f_T and f_{max} with the measured data over the entire range of measured w_t. Some discrepancies between the measurements and the calculations are due to the errors associated with the device process in pattern lithography. Because g_m and C_{gs} are both proportional to w_t, as shown in Eq. (2), f_T is not a function of w_t. From our calculations contained in Fig. 3, f_T showed an almost constant frequency of about 100 GHz above a w_t of about 100-μm. Below this w_t f_T showed a slight increase with w_t owing to the y-axis intercept effect of C_{gd}, as observed in many earlier studies [23, 24]. Since f_{max} is a strong function of R_g as shown in Eq. (3), it is affected by both N and w_t. If we assume that G_{ds} is negligible (ideal case without channel length modulation), Eq. (3) is simply expressed as [25]:

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi R_g C_{gd}}} \tag{14}$$

Because f_T is almost constant, we therefore obtain:

$$f_{\max} \propto \frac{1}{\sqrt{R_g(N, w_t) \cdot C_{gd}(w_t)}} \tag{15}$$

Eq. (15) shows that a careful combination of N and w_t is required to achieve a maximum f_{max} in a given device technology. Obviously, a greater w_t produces a higher f_{max}; however, to increase the number of gate-fingers by reducing the unit gate width is more efficient than to simply increase the single-gate_width in order to maximize f_{max} at a given w_t.

Ⅳ. Conclusion

We investigated the effects of N and w on the RF characteristics of 0.1-μm depletion-mode multi-finger MHEMTs and their small-signal parameters. C_{gs}, C_{gd}, G_{ds}, and $g_{m,int}$ were all proportional to w_t; however, R_i and R_s were inversely proportional to w_t. R_g was proportional to both w_t and $1/N^2$. f_T and f_{max} were calculated by using the small-signal models and curve-fitting equations from each extracted small-signal parameters. The calculations showed good agreements with the measurements, and the results demonstrated that a greater w_t produces a higher f_{max}; however, to maximize f_{max} at a given w_t, increasing the number of gate_fingers is more efficient than increasing the single-gate width. On the other hand, f_T showed an almost independent relationship with w_t. To our knowledge, this is the first successful demonstration of multi-finger gate-width scaling effects (individual effect of N and w_t) on HEMT devices operating at millimeter-wave frequencies.

This work was supported by the Industrial Strategic Technology Development Program (contract no. 10038766) funded by the Ministry of Knowledge Economy (MKE, Korea) through ETRI.

References

[1] Y. Cordier, S. Bollaert, M. Zaknoune, J. Dipersio, and D. Ferre, "InAlAs/InGaAs metamorphic high electron mobility transistors on GaAs substrate: influence of indium content on material properties and device performance," *Japanese Journal of Applied Physics*, vol. 38, no. 2B, pp. 1164-1168, Feb. 1999.

[2] K. Chang, I. Bahl, and V. Nair, "Power amplifiers," in *RF and Microwave Circuit and Component Design for Wireless Systems*, 1st ed. New York, NY: Wiley, 2002, pp. 405-406.

[3] M. Chertouk, H. Heiss, D. Xu, S. Kraus, W. Klein, G. Bohm, G. Trankle, and G. Weimann, "Metamorphic InAlAs/InGaAs HEMT's on GaAs substrates with a novel composite channels design," *IEEE Electron Device Letters*, vol. 17, no. 6, pp. 273-275, Jun. 1996.

[4] F. Medjdoub, S. Vandenbrouck, C. Gaquiere, E. Delos, M. Zaknoune, and D. Theron, "Power measurement setup for large signal microwave characterization at 94 GHz," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 4, pp. 218-220, Apr. 2006.

[5] L. Shen, S. Heikman, B. Moran, R. Coffie, N. Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "GaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Letters*, vol. 22, no. 10, pp. 457-459, Oct. 2001.

[6] D. Ducatteau, A. Minko, V. Hoel, E. Morvan, E. Delos, B. Grimbert, H. Lahreche, P. Bove, C. Gaquiere, J. C. De Jaeger, and S. Delage, "Output power density of 5.1/mm at 18 GHz with an AlGaN/GaN HEMT on Si substrate," *IEEE Electron Device Letters*, vol. 27, no. 1, pp. 7-9, Jan. 2006.

[7] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-volgate AlGaN/GaN HEMT for power electronics applications," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 356-362, Feb. 2006.

[8] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using field plate," *IEEE Transactions on Electron Devices*, vol. 48, no. 8, pp. 1515-1521, Aug. 2001.

[9] G. Meneghesso, A. Neviani, R. Oesterholt, M. Mat-

loubian, T. Liu, J. J. Brown, C. Canali, and E. Zanoni, "On-state and off-state breakdown in GaInAs/InP composite channel HEMT's with variable GaInAs channel thickness," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 2-9, Jan. 1999.

[10] Y. C. Chen, P. Chin, D. Ingram, R. Lai, R. Grundbacher, M. Barsky, T. Block, M. Wojtowicz, L. Tran, V. Medvedev, H. C. Yen, D. C. Streit, and A. Brown, "Composite-channel InP HEMT for W-band power amplifiers," in *Proceedings of the 11th International Conference on Indium Phosphide and Related Materials*, Davos, Switzerland, 1999, pp. 305-306.

[11] J. H. Lee, H. S. Yoon, C. S. Park, and H. M. Park, "Ultra low noise characteristics of AlGaAs/InGaAs/GaAs pseudomorphic HEMT's with wide head T-shaped gate," *IEEE Electron Device Letters*, vol. 16, no. 6, pp. 271-273, Jun. 1995.

[12] J. H. Oh, M. Han, S. W. Moon, S. G. Choi, Y. H. Back, J. K. Rhee, and S. D. Kim, "Radio frequency characteristics of multifinger 0.1 μm metamorphic high-electron-mobility transistors depending on number of gate fingers and gate width," *Japanese Journal of Applied Physics*, vol. 46, no. 10A, pp. 6503-6508, Oct. 2007.

[13] S. W. Chen, O. Aina, W. Li, L. Phelps, and T. Lee, "An accurately scaled small-signal model for interdigitated power P-HEMT up to 50 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 5, pp. 700-703, May 1997.

[14] S. J. Nash, A. Platzker, and W. Struble, "Distributed small signal model for multi-fingered GaAs PHEMT/MESFET devices," *IEEE MTT-S International Microwave Symposium Digest*, San Franscisco, CA, 1996, pp. 1075-1078.

[15] A. Caddemi, G. Crupi, and N. Donato, "A robust and fast procedure for the determination of the small signal equivalent circuit of HEMTs," *Microelectronics Journal*, vol. 35, no. 5, pp. 431-436, May 2004.

[16] C. Y. Chang and F. Kai, "High electron-mobility transistor," in *GaAs High-Speed Devices: Physics, Tecnology, and Circuit Applications.* New York, NY: Wiley, 1994, pp. 375-382.

[17] M. B. Das, "A high aspect ratio design approach to millimeter-wave HEMT structures," *IEEE Transactions on Electron Devices*, vol. 32, no.1, pp. 11-17, Jan. 1985.

[18] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions and Microwave Theory and Techniques*, vol. 36, no. 7, pp. 1151-1159, Jul. 1988.

[19] Y. Kwon, M. Tutt, G. I. Ng, D. Pavlidis, T. Brock, P. Marsh, J. Oh, J. Castagne, and N. T. Linh, "Gate-recess and device geometry impact on the microwave performance and noise properties of 0.1 μm InAlAs/InGaAs HEMT's," in *Proceedings of IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Ithaca, NY, 1991, pp. 141-150.

[20] C. Gaquiere, B. Bonte, D. Theron, Y. Crosnier, and, J. Favre, "Analysis of the source inductance effect on the power performance of high development HEMTs in the Ka-band," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 8, pp. 243-254, Aug. 1995.

[21] H. Rohdin, N. Moll, C. Y. Su, and G. S. Lee, "Interfacial gate resistance in Schottky-barrier-gate field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 45, no. 12, pp. 2407-2416, Dec. 1998.

[22] X. Jin, J. J. Ou, C. H. Chen, W. Liu, N. J. Deen, P. R. Cray, and C. Hu, "An effective gate resistance model for CMOS RF and noise modeling," *IEEE International Electron Devices Meeting (IEDM Technical Digest)*, San Francisco, CA, 1998, pp. 961-964.

[23] Y. C. Pao, C. Nishimoto, M. Riaziat, R. M. Ahy, N. G. Bechtel, and J. S. Harris, "Impact of surface layer on In/sub0.52/Al/sub0.48/As/In/sub 0.53/Ga/sub 0.47/As/InP high electron mobility transistors," *IEEE Electron Device Letters*, vol. 11, no. 7, pp. 312-314, Jul. 1990.

[24] J. H. Oh, Y. H. Baek, B. O. Lim, S. W. Moon, S. J. Lee, J. K. Rhee, I. S. Hwang, and S. D. Kim, "Effects of gate-recess structure on high frequency characteristics of 0.1 μm metamorphic HEMTs," *Journal of the Electrochemical Society*, vol. 154, no. 7, pp. H541-H546, Jul. 2007.

[25] N. I. Cameron, S. Murad, H. McLelland, A. Asenov, M. R. S. Taylor, M. C. Holland, and S. P. Beaumont, "Gate recess engineering of pseudomorphic In0.30GaAs/GaAs HEMTs," *Electronics Letters*, vol. 32, no 8, pp. 770-772, Apr. 1996.

Pil-Seok Ko

received a B.S. degree in Electronics Engineering from the Dongguk University, Seoul, Korea, in 2012. Also He is currently working toward the Master degree at the Department of Electronics and Electrical Engineering, Dongguk University, Seoul, Korea. His research interests include semiconductor fabrication and III-V semiconductor material.

Hyung-Moo Park

received the B.S degree in electronic engineering from Seoul National University, Seoul, Korea, in 1978. He also received the M.S. and Ph.D. degrees in electronic engineering form KAIST, Deajeon, Korea, in 1980 and 1984, respectively After he received the Ph.D. degree, he joined Electronics and Telecommunications Research Institute (ETRI), Deajeon, Korea, where he has been involved in the development of GaAs and InP High Electron Mobility Transistors (HEMTs). Since 2000, he has been a Professor in the division of Electronics and Electrical Engineering at Dongguk University.