J Electr Eng Technol Vol. 9, No. 1: 197-204, 2014
http://dx.doi.org/10.5370/JEET.2014.9.1.197

ISSN(Print)1975-0102
ISSN(Online) 2093-7423

Analysis, Design and Implementation of an Improved ZVZCS-PWM Forward converter

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Abstract – In this paper an Improved Zero Voltage Zero Current Pulse Width Modulation Forward converter which employs a simple resonance snubber circuit is introduced. A simple snubber circuit consists of a capacitor, an inductor and two diodes. In proposed converter, switch Q1 operates at ZCS turn-on, and ZVS turn-off conditions and all-passive semiconductor devices operate at ZVZCS turn-on and turn-off state. The proposed converter is analyzed and various operating modes of the ZVZCS-PWM forward converter are discussed. Analysis and design considerations are presented and the prototype experimental results of a 100w (40 V/2.5A) proposed converter operating at 30 KHz switching frequency confirm the validity of theoretical analysis.

Keywords: Forward converter, Pulse width modulation, Zero voltage switching, Zero current switching, TL494.

1. Introduction

Pulse width modulated (PWM) forward converter is used in industry in a wide variety of applications. This converter is required to operate with high switching frequencies due to demands for small converter size and high power density. High switching frequency operation, however, results in higher switching losses, increased electromagnetic interference (EMI), and reduced converter efficiency. Numerous soft-switching techniques have been proposed to correct these problems [1-17]. Almost all these techniques achieve soft switching condition in the main switch using an active auxiliary circuit. Some of these active auxiliary circuits are resonant tanks are added to the conventional converters. Quasi-resonant converters are a type family of these converters, that introduced in reduce the switching losses in PWM converters operating at high switching frequency. In these converters, resonances occur in the switch current or in the voltage across the switch [1-7]. In Quasi-resonant converter, switching losses are significantly reduced, but in these types of converters, voltage and current stresses occur.

In [8-10] proposed converter designed to limit the voltage stresses of switches, and the switches can be turned on at the zero-voltage switching (ZVS) during the transition interval.

However, the reverse recovery problem of the rectifier diode will result in the serious spike voltage across the diode.

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Received: February 15, 2013; Accepted: August 26, 2013

For improving these problems, various forms of soft-switching techniques for forward converter have been proposed [11-13].

They have been removing the conventional reset winding in switching transformer and achieving soft switching. In [11], converter must operate at frequency modulation and output filter is not optimum.

In [12] an auxiliary transformer is used to achieve soft-switching, and It results in difficultly and complexly designing. In order to improving these problems in converters, zero-voltage transition (ZVT) and zero-current transition (ZCT) converters are developed [13-16]. ZVT and ZCT converters have the advantages of resonant and quasi-resonant converters like low EMI, and the resonances are limited with switching instances, and therefore the converter operates like a regular PWM converter, but in these converters, an auxiliary circuit containing resonant elements and auxiliary switches are used, and need complexity control system.

The aim of this paper is to introduce a simple snubber cell for dc/dc PWM forward converters. The circuits scheme of the new zero voltage and zero current switching pulse width modulation forward converter is shown in Fig. 1. The ZVZCS technique in this paper is provided by a snubber cell. The snubber cell consists of a resonant inductor Lr , a resonant capacitor Cr and two diodes Dr and D . The switch $Q1$ in the proposed converter turn on at zero current switching (ZCS), and turn off at zero voltage-zero current switching (ZVZCS without any voltage or current spikes on switch and diodes.

To simplify the steady-state analysis of the circuit given in Fig. 1 during one switching cycle, it is assumed that input and output voltages and output current are constant, and semiconductor devices and resonant circuit are ideal.

The main theoretical waveforms of the proposed forward

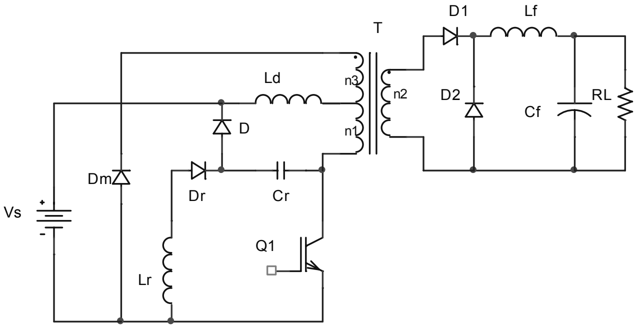


Fig. 1. Proposed ZVZCS-PWM forward converter

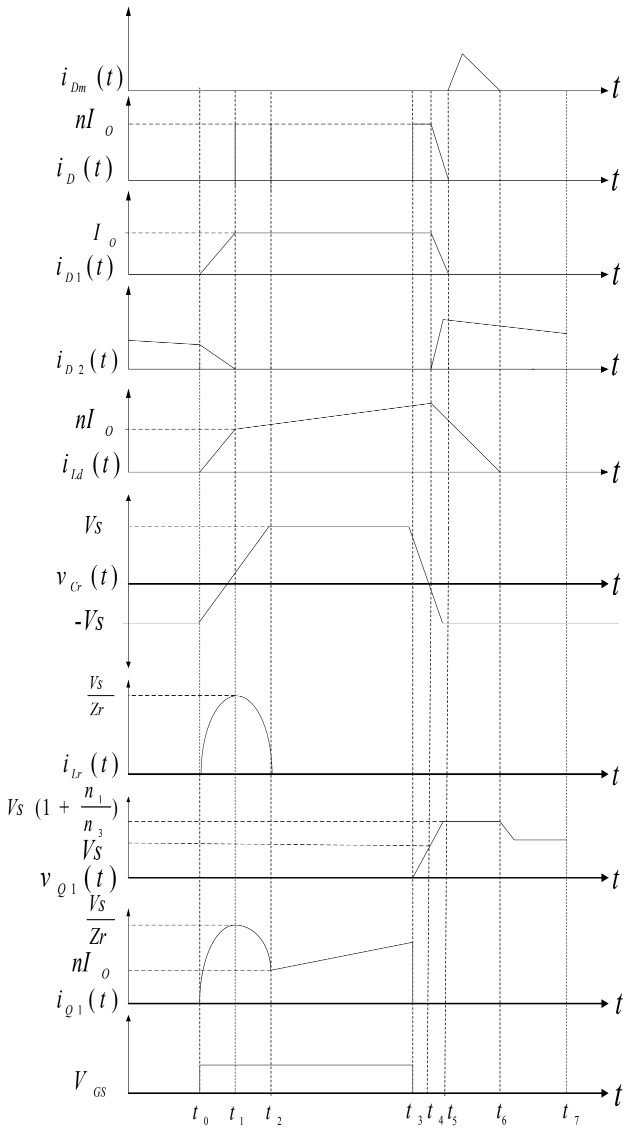


Fig. 2. Theoretical waveforms

converter are shown in Fig. 2, and the equivalent circuit for each operating interval is shown in Fig. 3.

The theoretically analyzed of proposed ZVZCS converter is in Section 3. The output characteristics of converter and design guideline are presented in Section 4. In Section 5, analysis and design considerations verify by the prototype experimental results of a 100W (40 V/2.5A) proposed converter operating at 30 KHz switching frequency.

2. Proposed ZVZCS - PWM Converter

In the classical configuration of forward converter, a major disadvantage of the reset winding is that the transformer leakage inductance discharge spike cannot be put off. The leakage spike causes a high voltage stress across the power switch, and another disadvantage is the hard turn off of power switch. Both of them decrease the efficiency of power forward converter. In this paper a lossless snubber for the single switch forward converter is proposed, as

1. Absorbs the leakage inductance energy.
2. Provides zero current switching for power switch at turning on state.
3. Control switch dv/dt at turning off state, thus Provides zero voltage switching for power switch.
4. Removes the high voltage stress across the power switch at turning off state.
5. Provides the soft switching (ZVS or ZCS) turn on and turn off for all semiconductor devices in forward converter.

3. Operation Principles and Analysis

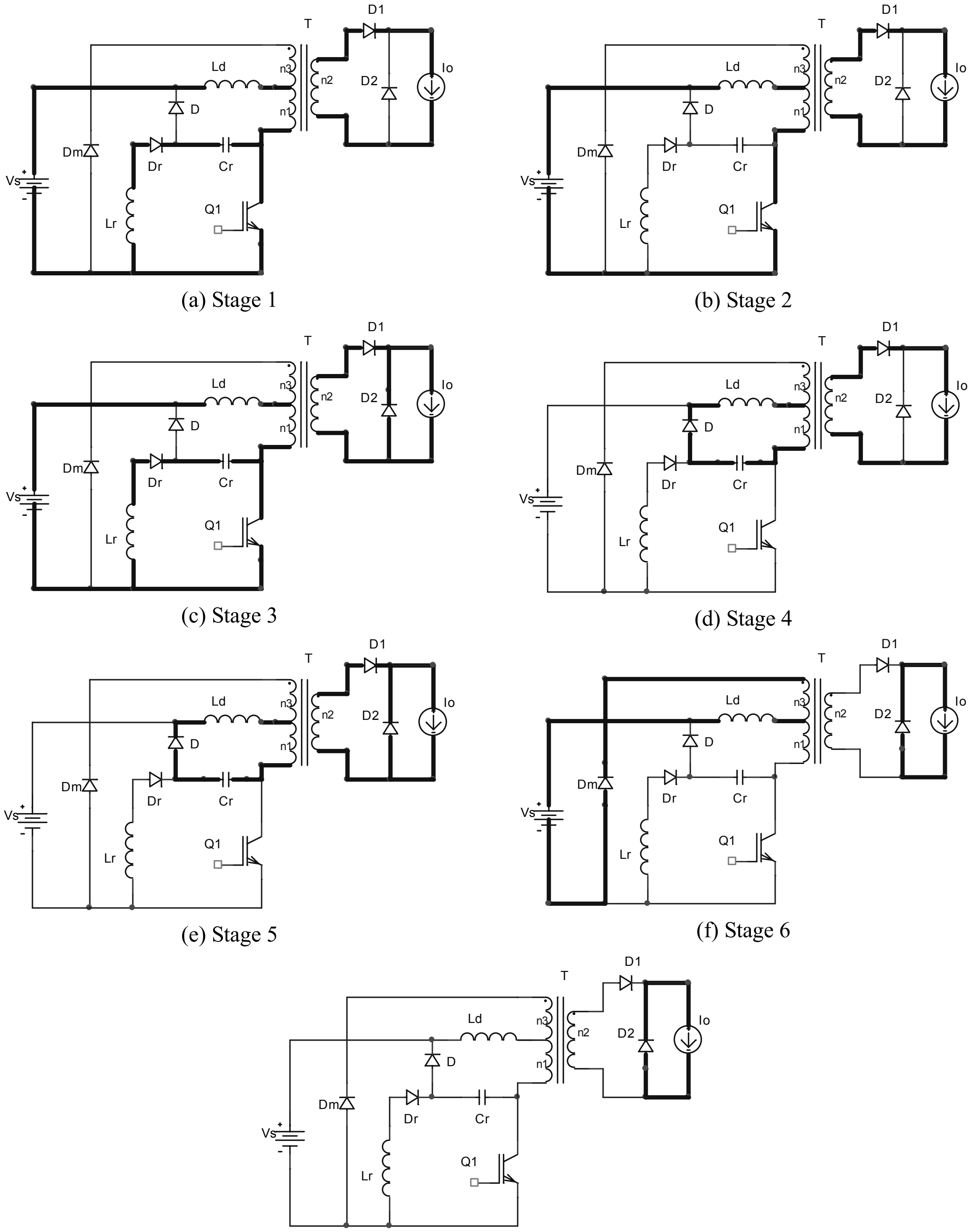
Seven stages occur within one switching cycle in the steady state operation of the proposed converter. The equivalent circuit schemes of these operation stages are given in Fig. 3(a)-(g), respectively.

Stage 1 [t_0, t_1 : Fig. 3(a)]: At the beginning of this stage, the switch Q1 is in the off state. The free- wheeling diode D2 is in the on state and conducts the load current I_o. At earlier moment of $t = t_0$, the equations $V_{cr} = -V_s$ and $I_{Lr} = I_{Ld} = 0$ are valid.

At $t = t_0$, turn on signal is applied to the gate of the main IGBTs Q1 and it turns on under exactly ZCS through leakage inductor Ld. In this stage the resonance between Cr and Lr occurs through diode Dr, and resonance capacitor Cr begins to discharge on the resonance inductor Lr and resonance inductor current $i_{Lr}(t)$ increases. During this stage, currents of main switch Q1 rises and D2 current falls simultaneously and linearly. Thus, the Eq. (1) can be written for switch current.

$$i_{Ld}(t) = \frac{Vs}{Ld}(t - t_0) \tag{1}$$

The resonant inductor current and resonant capacitor voltage can be written as follow in this interval.



(a) Stage 1
(b) Stage 2
(c) Stage 3
(d) Stage 4
(e) Stage 5
(f) Stage 6
(g) Stage 7

Fig. 3. Equivalent circuit schemes of the operation stages in the proposed converter

$$i_{Lr}(t) = \frac{V_s}{Z_r} \sin \omega_r (t - t_0) \tag{2}$$

$$v_{Cr}(t) = -V_s \cos \omega_r (t - t_0) \tag{3}$$

Where

$$Z_r = \sqrt{Lr / Cr} \tag{4}$$

And

$$\omega_r = 1 / \sqrt{Lr.Cr} \tag{5}$$

At $t = t_1$, D1 current reaches to the load current I_o, and switch current reaches to primary reflected output current nI_o that $n = n_2 / n_1$, and D2 current falls to zero and turns off under exactly ZVZCS, and this stage finishes.

The time interval Δt_1 of this stage is written as follow.

$$\Delta t_1 = t_1 - t_0 = \frac{n.I_o.Ld}{Vs} \tag{6}$$

Stage 2 *[t_1, t_2 :Fig. 3(b)]:* In this stage, load current flows through D1, and the reflected current nI_o plus magnetic current of transformer flows through switch Q1. At $t = t_1$ the resonance between Cr and Lr continues in stage 1. During this stage the resonant voltage $v_{Cr}(t)$ decreases firstly, then after cross of zero reaches to V_s and the resonant current $i_{Lr}(t)$ decreases from its peak, and reaches to zero at $t = t_2$, and Dr turns off under ZVZCS, and this state finishes.

The resonance $i_{Lr}(t)$ and $v_{Cr}(t)$ can be described, respectively as follow.

$$i_{Lr}(t) = \frac{V_s}{Z_r} \sin \omega_r (t - t_1) \tag{7}$$

$$v_{Cr}(t) = V_s \cos \omega_r (t - t_1) \tag{8}$$

The time interval of this stage is given by Eq. (9).

$$\Delta t_2 = t_2 - t_1 = \frac{\pi}{\omega_r} - \Delta t_1 \tag{9}$$

Stage 3 *[t_2, t_3 :Fig. 3(c)]:* This stage is on state of the conventional PWM forward converter and, power transfer process occurs from source to load. During this stage, the primary transformer current $i_{Ld}(t)$ increases and $i_{Lr}(t)$ and $v_{Cr}(t)$ can be written, respectively, as follow.

$$i_{Lr}(t) = i_{Dr} = 0 \tag{10}$$

$$v_{Cr}(t) = V_s \tag{11}$$

At $t = t_3$, switch Q1 turn off under ZVS condition due to capacitor charge, and diode D turns on under ZVZCS and this stage finishes. The time interval Δt_3 of this stage is written in Eq. (12).

$$\Delta t_3 = DT_s - \Delta t_2 - \Delta t_1 \tag{12}$$

Where D is the duty cycle of control signal and $T_s = 1 / f_s$ is the switching period. f_s is the switching frequency.

Stage 4 *[t_3, t_4 :Fig. 3(d)]:* At $t = t_3$, the switch Q1 turns off under ZVS, and diode D turns on and conducts the reflected load current nI_o. At $t = t_4$ resonance capacitor Cr discharge on Ld and resonance capacitor voltage reaches to zero value, and allowing diode D2 start to conduct.

The resonant $v_{Cr}(t)$ for this interval is derived as follow.

$$v_{Cr}(t) = -\frac{n.I_\circ}{Cr}(t - t_3) + V_s \tag{13}$$

The time interval of this stage is written as follow.

$$\Delta t_4 = t_4 - t_3 = \frac{V_s.Cr}{n.I_\circ} \tag{14}$$

Stage 5 [t_4, t_5 :Fig. 3(e)]: At $t = t_4$, the diode D2 begins to conduct and the resonance between leakage inductance Ld and capacitor Cr begins, and Cr charges by Ld. During this stage the resonant current $i_{Ld}(t)$ decreases from its peak value and $v_{Cr}(t)$ arrives to $-V_s$ at $t = t_5$, and then, diode D turns off. The resonant $i_{Ld}(t)$ and $v_{Cr}(t)$ can be described, respectively as follow.

$$I_{Ld}(t) = n.I_o.\cos \omega_d (t - t_4) \tag{15}$$

$$v_{Cr}(t) = -\frac{n.I_o}{Z_d} \sin \omega_d (t - t_4) \tag{16}$$

Where

$$Z_d = \sqrt{Ld / Cr} \tag{17}$$

And

$$\omega_d = 1 / \sqrt{Ld.Cr} \tag{18}$$

At $t = t_5$, $v_{Cr}(t)$ arrives to $-V_s$, and diodes Dm turns on under ZVZCS and this stage finishes.

The time interval of this stage is written as follow.

$$\Delta t_5 = \frac{1}{\omega_d} \arcsin\left(\frac{V_s.Z_d}{n.I_o}\right) \tag{19}$$

Stage 6 [t_5, t_6 :Fig. 3(f)]: At $t = t_5$, transformer starts with the beginning of reset through diode Dm. At $t = t_6$, $i_{Dm}(t)$ nulls to zero, and transformer resets completely. The $v_{Cr}(t) = -V_s$, and $i_{Ld}(t)$ decreases during this interval, and $i_{Ld}(t)$ can be described as follow.

$$I_{Ld}(t) = -\frac{V_s}{Ld}(t - t_5) + I_{Ld}(t_5) \tag{20}$$

The time interval of this stage is written a follow.

$$\Delta t_6 = t_6 - t_5 = \frac{I_{Ld}(t_5).Ld}{V_s} \tag{21}$$

Stage 7 [t_6, t_7 :Fig. 3(f)]: This stage at $t = t_6$ starts when freewheeling diode D2 current reaches to the load current. At $t = t_7$, one switching cycle is completed and another switching cycle begins.

4. Design Procedure

4.1. DC voltage transfer function

The voltage conversion ratio is derived by equating the average output voltage per cycle. In steady state operation, can be described average output voltage as follow.

$$Vo = \frac{1}{Ts}\int_0^{Ts} v_{cf}(t)\,dt = \frac{1}{Ts}\left[\int_{t_1}^{t_2} nV_s + \int_{t_2}^{t_3} nV_s + \int_{t_3}^{t_4} nv_{Cr}(t)\right] \quad (22)$$

$$Vo = nV_s(DT_s\text{-}\Delta t_1)\text{-}\frac{n^2 I_o}{2C_r}\Delta t_4^{\,2} + nV_s\Delta t_4 \quad (23)$$

From Eqs. (6) and (14) the expression for the conversion ratio can be calculated as follow

$$M = \frac{Vo}{Vs} = D.n - \frac{f_s}{2\pi f_d}\left[M.Q.n^2 - \frac{1}{2MQ}\right] \quad (24)$$

Where M is dc conversion ratio, $Q = Z_d / R_L$ is normalized load and D is duty cycle of switches and $D = (\Delta t_1 + \Delta t_2 + \Delta t_3)/T_s$. Fig. 4 shows the voltage conversion ratio $M = V_o / V_s$ versus the normalized load Q, for different values of duty ratio D, a fixed normalized frequency $f_s / f_d = 0.15$ and n = 1, where $n = n_2 / n_1$ is turns ratio of transformer, f_s is switching frequency and f_d is resonance frequency.

The proposed ZVZCS PWM forward converter is designed for the following specifications.

The input data are defined as follows:

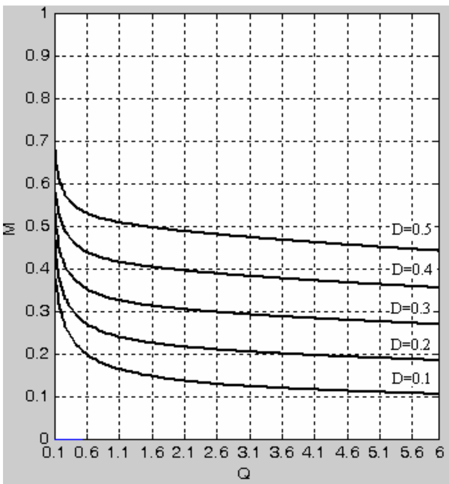


Fig.4. M Versus Q with different D, and fixed f_s / f_d = 0.15

- Output power: $P_o = 100W$;
- Output voltage: $V_o = 40V$;
- Input voltage: $V_s = 100V$;
- Load resistance: $R_L = 16\Omega$;
- Switching frequency = 30KHz;

4.2. Design transformer and output filter

Although the lossless snubber cell is present in the PWM forward converter, the transformer turns ratio and output filter can be selected using the traditional hard switching forward converter design method [18] as follow:

$$n = \frac{n_2}{n_1} = \frac{M}{\eta.D_{\max}} = \frac{0.4}{0.9*0.5} = 0.89$$

Where η is the efficiency of converter, and we are assumed $\eta = 0.9$. $D_{\max}$ is maximum value of the duty cycle and $D_{\max} = 0.5$ is selected with reference to [19]. $n = 1$ is selected. Ferrite E 42/33/20 core is selected as transformer , core and $n_1 = n_2 = n_3 = 40$ turns.

The filter inductor L_f and filter C_f capacitor are designed like a regular PWM forward converter. Voltage output ripple and current output ripple must not exceed 1 and 20 percent respectively.

$$L_f = \frac{V_o(\text{1-D})}{\Delta I_{Lf}.f} = 4mH, \quad C_f = \frac{\text{1-D}}{8.L_f.\frac{\Delta V_o}{V_o}.f^2} = 2\mu F$$

4.3 Design the snubber parameters

The snubber capacitor is designed to control dv/dt of the drain to source voltage of the power switch. When the main switch turns off, it provides an alternative path for the leakage inductance current to reduce switching turning OFF losses and dv/dt EMI noises.

The snubber inductor L_r and the snubber capacitor C_r can be selected using the Fig. 4. From Fig. 4, the normalized load $Q = 1.5$ for $M = 0.4$ and $D = 0.4$, is obtained, then $Z_d = Q.R_L = 24\Omega$. According to the Eq. (4) and Eq. (5) can be calculated L_r and C_r as follow.

$$Lr = Ld = \frac{Z_d}{\omega_d} = 19\mu H, \quad Cr = \frac{1}{Z_r.\omega_r} = 33nF$$

In order to minimize the influence of the resonant parameters and to easily achieve ZVS turning-OFF for power switch, we are selected $f_s / f_r = 0.15$. Thus

$$\omega_r = \omega_d = 2\pi f_d = 2\pi.\frac{30}{0.15}.10^3 = 2\pi * 200 * 10^3 (rad/s)$$

5. Experimental Results

The complete circuit diagram of the proposed converter is shown in Fig. 5.

The control system implemented by two main IC that, they are TL494 and IR2110. The output pulse of the TL494 PWM controller is applied to IR2110. TL494 used for control output voltage, and produces PWM pulse signal. The IR2110 is high voltage, high speed power MOSFET driver with independent high and low side referenced output channels. The output pulse of LO pin is applied to gate of power switch $Q1$. By this control circuit, at converter nominal duty cycle is applied to the switch.

In Figs. 6-8 and 9 show the some obtained experimental results of the prototype proposed converter from Fig. 5.

Fig.6 is shown voltage and current of the switch $Q1$. In Fig. 6, it can be noticed that power switch in proposed converter operates at ZCS and ZVS mode respectively at turning on, and turning off, and it can be noticed that $Q1$ don't have any voltage and current spikes in switching state.

Fig. 7, is shown the current of resonant inductor $i_{Lr}(t)$, the Leakage inductor current $i_{Ld}(t)$ and resonant capacitor voltage $v_{Cr}(t)$. As Fig. 7 can be seen the experimental waveforms are closed to theoretical waveform, and confirming the soft switching without voltage and current stresses.

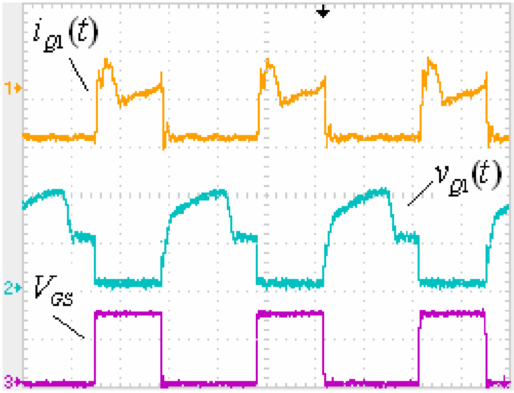


Fig. 6. voltage and current of switch $v_{Q1}(t) = 100V/div$, $i_{Q1}(t) = 3A/div$, $V_{GS}(t) = 10V/div$ $time: 10\,\mu s/div$

Fig. 8 is shown output voltage V_O and output current I_O.

As experimentally results of ZVZCS PWM forward converter, it can be clearly seen that the predicted operation principles and theoretical analysis are verified.

The losses of the converter components used for experimental verification are calculated based on formulas at [18, 20] at full load condition, and are listed in Table 1.

The experimentally efficiency curve of the converter versus output power shows in Fig.9. Notice that proposed converter has 92% efficiency in full load, and also has high

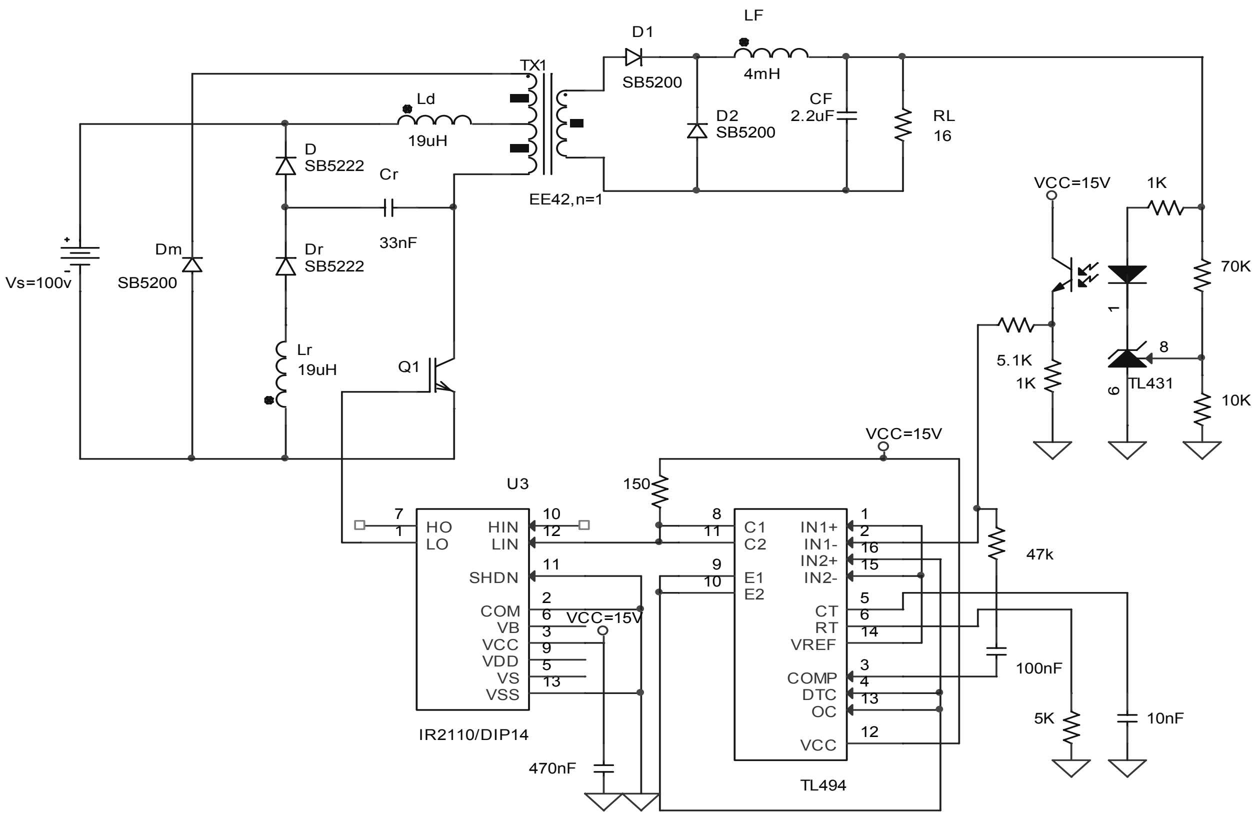


Fig. 5. Complete circuit of the implemented prototype

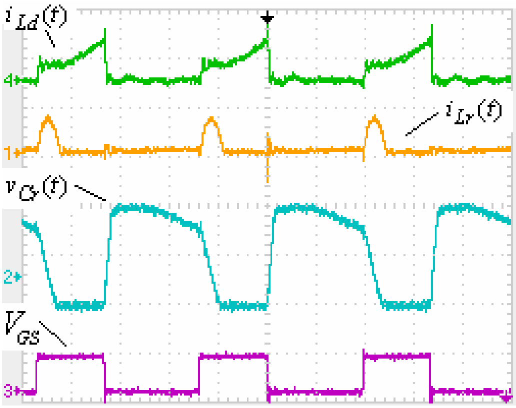


Fig. 7. $i_{Lr}(t) = i_{Ld}(t) = 5A/div$, $v_{Cr}(t) = 100V/div$, $V_{GS}(t) = 20V/div$, $time: 10\,\mu s/div$

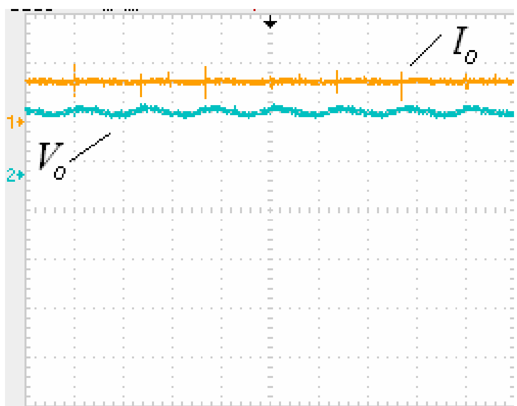


Fig. 8. Output voltage V_o and output current I_o $V_0 = 20V/\ div$, $I_0 = 1A/div$

Table 1. Comparison of power losses of the proposed converter and the conventional converters

	Proposed converter Losses(w)	Conventional converter Losses (w)
IGBT conduction loss	1.388	1.262
IGBT switching loss	0	8
Diode D_1 losses	1.228	1.228
Diode D_2 losses	1.228	1.228
Diode D_r losses	0.201	0
Diode D losses	0.096	0
output inductor ESR loss	0.312	0.312
Secondary winding loss	0.582	0. 582
Primary winding loss	0.817	0.743
Filter capacitor ESR loss	5m	5m
Snubber inductor ESR	8m	0
Core transformer loss	1.55m	1.55m
Efficiency	0.94	0.88

efficiency in light load.

At proposed converter the conduction losses in the IGBT around 10% is higher than conventional hard switching converter, due to its peak current.

$I_0 = 1A/div$

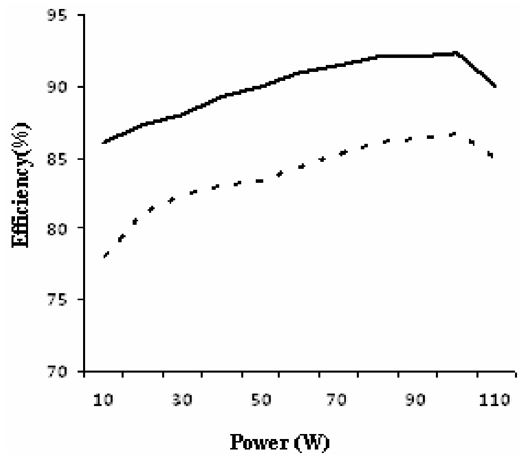


Fig. 9. Efficiency of the proposed converter (continuous line) and hard switching counterpart (broken line) versus output power

6. Conclusion

In this paper Improved Zero Voltage Zero Current Pulse Width Modulation (ZVZCS-PWM) Forward converter which employs a simple snubber circuit that overcomes most of the drawbacks of the normal PWM dc-dc forward converter is proposed. The switch Q1 operates at ZCS turn-on and ZVS turn-off, and the all-passive semiconductor devices operate at soft switching turn-on and turn-off. This new converter has no additional current and voltage spikes and conduction loss in the main switch in comparison to the hard-switching converter counterpart and is suitable for high switching frequency and high power operation. A PWM ZVZCS forward converter with has been analyzed in detail. The predicted operation principles and theoretical analysis of this converter has been exactly verified with experimental results of a 100W and 30KHz IGBT-PWM proposed converter. It has been clearly observed that power switch have operated with soft switching.

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