J Electr Eng Technol.2017; 12(2): 522-532
https://doi.org/10.5370/JEET.2017.12.2.522

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Fault Analysis Method for Power Distribution Grid with PCS-based Distributed Energy Resources

Dong-Eok Kim† and Namhun Cho*

Abstract – In this study, we propose a fault analysis method for a power distribution grid with PCS-based DERs. We first explain the characteristics of a PCS-based DER. According to the characteristics, the DER is considered as a current-controlled voltage source, which produces varying voltages within a certain limit so that currents equal to given references flowing from the DER to the grid (currents controlled). So, we introduce the symmetrical equivalent models in the form of varying voltage source for fault analysis and then, construct a convex optimization problem to solve the fault problem associated with the equivalent models and grid conditions. Thus, the proposed method enables to perform a proper fault analysis considering the characteristics of the DER, which are currents controlled, voltage limited, and unity power factor achievement. To verify the validity of the proposed method, we perform computer simulations with the proposed method and with MATLAB Simulink, and the results are compared.

Keywords: Fault analysis, Power conversion system, Distributed energy resources

1. Introduction

With advanced power conversion technologies with power electronics, many distributed energy resources (DERs) with power conversion systems (PCSs) have been developed and integrated into the power distribution grid. The impact of distributed energy resources on the power grid has been discussed in several studies [1-4]. However, as a PCS-based DER has different structure and control strategy from those of a conventional system [5], its impact on the power grid requires a different approach and analysis.

Conventional distributed power sources integrated to the grids by synchronous generators (SGs) with small internal impedances have excitation systems to maintain the rotor voltage at given values, they were considered as voltage sources. On the other hand, a PCS-based DER includes a DC/AC power converter, which is often called an inverter, to integrate an energy resource into the power grid. The inverter converts DC to AC by chopping the DC voltage with a PWM technique; thus, it produces a large amount of switching noise. As the noise from a PCS-based DER to the power grid should be less than a certain amount, the inverter includes a comparatively large filter inductance to eliminate the noise [6]. In addition, the inverter uses feedback current control schemes for a stable power flow from the energy resource to the grid [7], especially for intermittently changing renewable energy resources. For these reasons, a PCS-based DER is considered to be a current source [8] when analyzing its effect on the power grid. Here, it must be recalled that power system analysis results would be totally different by what type of sources we apply among voltage and current sources.

As a result of the feedback control of the inverter current, the inverter causes some over-voltage phenomena under various abnormal conditions such as a load-rejection or single-line fault. In [9], experimental tests were performed to observe the transient characteristics of commercial inverter systems when a load is suddenly disconnected. Moreover, the authors of [10] extended the test to the case in which these systems are islanded. However, these studies are only demonstrated their tendencies when reacting to transients for the given conditions. In [11], a single-line fault in a power grid including a PCS-based DER was analyzed, but the DER was assumed to be an ideal current source, which implies that the inverter voltage unrealistically increases in some cases.

It is important to note that the inverter basically generates an AC voltage from a DC source; that is, the inverter is a variable voltage source. Current control is carried out by varying the inverter voltage, and the voltage is limited by a control limit [12] or some other means depending on the grid conditions. Therefore, in order to analyze the impact of a PCS-based DER on the power grid properly, we must consider the characteristics of both the current source and varying voltage source, including the effects of the voltage limit.

In this study, we propose a fault analysis method for a power distribution grid with PCS-based DERs. We first introduce PCS-based DER's characteristics. Second, we derive DER's equivalent static source models based on

† Corresponding Author: KEPCO Research Institute, Korea Electric Power Corporation, Daejeon, Korea. (cscotop@hanmail.net)
* KEPCO Research Institute, Korea Electric Power Corporation, Daejeon, Korea. (77ncho@gmail.com)
Received: July 18, 2016; Accepted: November 22, 2016

these characteristics. Then, we construct a convex optimization problem to solve the fault problem associated with the DER's equivalent models as well as the grid conditions. To verify the validity of the proposed method, we perform computer simulations with the proposed method and with MATLAB Simulink, and the results are compared.

It is highlighted that the proposed method enables to analyze the effects to the grid with PCS-based DERs applying 1) current controls, 2) inverter output voltage limits, and 3) unity power factor achievement at point of interconnection, without complicated and time-consuming dynamic simulations. In addition, we remind the readers that the analysis results are valuable because they are used to confirm if the grid effective grounding remains when fault occurs and to choose proper transient voltage surge suppressors (surge arrestors) for the protection of power equipment in the grid.

2. PCS-based DER

A steady-state fault analysis for a power distribution grid is generally performed with static source models. To derive an appropriate static source model for a PCS-based DER to conduct a fault analysis, it is important to comprehend the operating characteristics. In this paper, "DER" will mean "PCS-based DER" unless otherwise noted.

2.1 Operating characteristics

A DER roughly consists of two parts: the renewable energy sources with power converters in Fig. 1(a) and the inverter system for grid integration in Fig. 1(b). The renewable energy sources require power converters to convert AC power to DC power or to change the magnitude of the DC voltage. Assuming that the losses of the power converters are ignored, this part can be equivalently reduced to a variable current source as follows:

$$I_{RN}(t) = P_{RN}(t)/V_{DC}(t), \tag{1}$$

where P_{RN} is the randomly generated power from the renewable source, and V_{DC} is DC-link voltage.

The inverter system has four parts: the 1) DC-link part, 2) DC/AC-converter part, 3) LCL-filter part, and 4) control part. First, the DC-link part acts as a buffer to maintain the DC-link voltage within certain range for a short time when the power from a renewable energy source and the power to the grid through the inverter system are unbalanced. This part might include additional resistors connected to a DC link to resolve a power unbalance. The DC-link voltage dynamics are expressed as

$$\frac{dV_{DC}(t)}{dt} = \frac{1}{C_{DC}V_{DC}(t)}\left(P_{RN}(t) - P_R(t) - P_{INV}(t)\right). \tag{2}$$

From (2), for $P_R = 0$, if DC-link voltage is maintained at a constant value by some control, i.e., $\dot{V}_{DC} \approx 0$, the power generated by the renewable energy source can be fully delivered to the grid through the inverter system.

Second, the DC/AC-converter part consists of power electronics switches with gate drivers. Its role is to generate AC voltages according to the given references by chopping the DC-link voltage. The chopping process is basically carried out with a sinusoidal pulse-width modulation (SPWM) technique [13]. The output voltages of the DC/AC converters appear as chopped pulse waveforms, which consist of the fundamental and switching frequency components. In the PWM process, the fundamental components of the output line-to-line voltage cannot exceed the DC-link voltage instantaneously, i.e.,

$$V_{INVas}(t) = \min(V^*_{INVas}(t), M_I V_{DC}(t)), \tag{3}$$

where $y = \min(x_1, x_2)$ means that y is equal to the smaller value of either x_1 or x_2, and M_I is the modulation index. The subscript *as* signifies the respective A-phase component represented in the stationary frame. The output voltages $V_{INVabcs}$ are floating because they are based on the DC-link neutral point "n." Regarding the limits of the voltage magnitude, (3) can be re-expressed in terms of the *dq* components in the rotating frame as

$$|V_{INV}| = \min(|V^*_{INV}|, M_I V_{DC}), \tag{4}$$

where $V_{INV} = V_{INVd} + jV_{INVq}$, and $V^*_{INV} = V^*_{INVd} + jV^*_{INVq}$. For simplicity, the notation (t) is omitted afterwards. The subscripts d and q signify the respective *d*- and *q*-axis

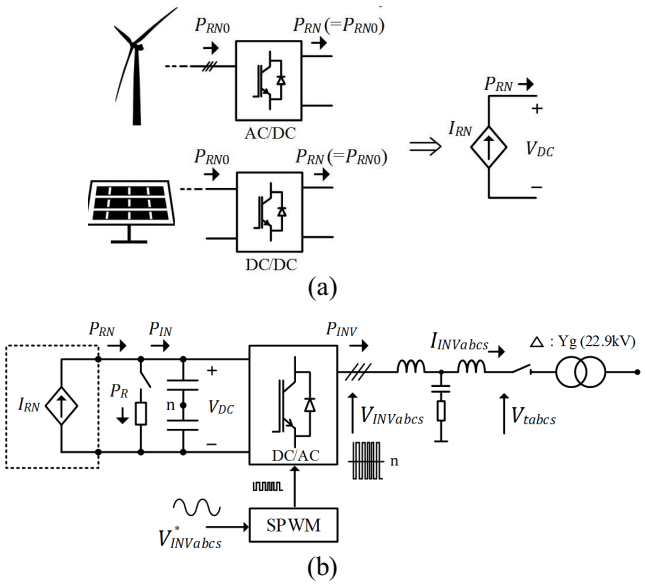

Fig. 1. Structure of a PCS-based DER structured consisting of (a) renewable energy sources with power converters and (b) an inverter system for grid integration

components represented in the *dq* (rotating) frame. It is noted that the *dq* components in the rotating frame are transformed with a *dq* transformation matrix from three phase components in the stationary frame [14], and it is assumed that all variables are represented per unit in this work to avoid confusion.

Third, the LCL filters consist of filter inductors, capacitors, and damping resistors. The LCL filters eliminate the switching frequency components so that the power related the fundamental frequency components is delivered to the grid. As the filter capacitance is typically very small and the damping resistance is quite large, the currents flowing into the capacitors are very small. Thus, for the steady-state analysis of the fundamental frequency, the capacitors and damping resistors can be ignored [6]. Then, the steady-state voltage equation for the filters in the *dq* frame is simply expressed with aggregated filter reactance X as follows:

$$V_t = V_{INV} - jXI_{INV}, \tag{5}$$

where $V_t = V_{td} + jV_{tq}$, and $I_{INV} = I_{INVd} + jI_{INVq}$. It is noted that a vector represented in the *dq* frame is the same as that represented in the phasor; thus, the relationship in (5) is also true in the phasor representation.

Fourth, the inverter system controls V_{DC} and the inverter (output) currents I_{INV}, as shown in Fig. 2. This control is generally performed in the synchronous rotating *dq* frame in which the *d* axis is aligned with the positive sequence components of the terminal voltage; this alignment — so-called synchronization — is achieved with a phase-locked loop (PLL) technique [7, 15]. In the synchronized frame, the active and reactive powers to the grid can be regulated by *d*- and *q*-axis current control, respectively; thus, the DC-link voltage is regulated by controlling the *d*-axis current

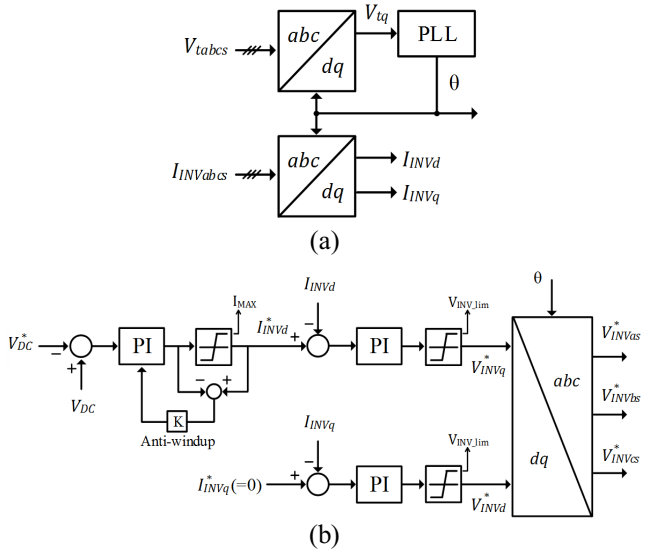

Fig. 2. Control part of the inverter system: (a) PLL controller; (b) DC-link and inverter current controllers

[16]. The *q*-axis current is generally controlled to zero to achieve a unity power factor. The outputs from the *d*- and *q*-axis current controllers are the *d*- and *q*-axis voltage references after the respective limiters, which implies

$$|V_{INV}^*| \le \mathrm{V_{INV\_MAX}}, \text{ where } \mathrm{V_{INV\_MAX}} = \sqrt{2}\,\mathrm{V_{INV\_lim}}. \tag{6}$$

And, the controller outputs are transformed into three phase components and used as the references for comparison with saw-tooth waveforms for the SPWM process. Again, it is important to note that the voltage references are equal to the inverter (output) voltages, except for the switching frequency components.

2.2 Setting the operating limits

Under the normal condition for a distribution grid, the power from the DER system is absorbed by the local loads or flows into the main source (substation side); thus, the inverter currents will be close to the rated current. On the other hand, when a fault occurs and the main source is active in the distribution grid, the magnitude of the positive sequence components of the voltage at the integration terminal decreases; therefore, the current should increase to have the same power before the fault flowing to the grid. However, the current cannot increase beyond the control limit; thus, the current remains at the limit, and the excess power is dissipated by the DC-link resistors. As an example of choosing the current limit, we consider IEEE Standard 1547. According to this standard, it is considered normal condition if the voltage at the integration terminal is greater than 88% and less than 110% of its rated value. This implies that the inverter current should be able to flow 113.6% more than its rated value at the rated power condition:

$$\mathrm{I_{MAX}} = 1.136\mathrm{K_1 I_{RATED}}, \tag{7}$$

where $\mathrm{K_1}$ is set to be equal to 1 unless the corresponding maximum current is stated in the specifications of the inverter system.

In addition, when a fault occurs, it is possible that the voltage at the integration terminal significantly increases. In this case, the inverter voltage should also increase so that the current is the same as that before the fault. However, this is unlikely because the inverter voltage is limited by both the respective controller limiters and DC-link voltage. The voltage limit in the control is similarly chosen as that in (7); it is normal unless the voltage at the integration terminal exceeds 110% of the rated value, and in this case, the current will be 91% of its rated value. Assuming that a unity power factor is achieved by the control, the following voltage limit is chosen:

$$\mathrm{V_{INV\_MAX}} = \mathrm{K_2}\left|1.1V_{t\_\mathrm{RATED}} - jX(0.91I_{INV\_\mathrm{RATED}})\right|, \tag{8}$$

where K_2 is set to be equal to 1 unless the corresponding maximum voltage is stated in the specifications of the inverter system. Finally, from (4), (6), and (8), we can expect the inverter voltage to be limited as

$$|V_{INV}| \le V_{lim} \text{ where } V_{lim} = \min(M_I V_{DC}, V_{INV\_MAX}). \quad (9)$$

2.3 Simplified model

For simplicity, we assume that the current control is carried out in some *dq* frame, not the synchronous *dq* frame in which the *d* axis is aligned with the integration terminal voltage, and that the phase of the current reference I^*_{INV} is properly obtained to achieve a unity power factor, which means that the *q*-axis component of the reference is not zero. Then, a DER can be represented in a simple form, as shown in Fig. 3. This simplified model can also be converted into a current source model (Fig. 4), which is useful in some fault cases.

2.3.1 DER's current source model

When the power factor at the integration terminal is controlled at 1, we can assume that a load resistance R_L is connected at the terminal. Moreover, considering that the control is carried out with simple PI controllers, the simplified model of the DER can be converted into a static current source model, where the current reference becomes the Norton current source, and the Norton impedance is written as

$$Z_{nt} = \frac{R_L}{R_L + jX}\left(K_P - j\frac{K_I}{\omega_c}\right), \quad (10)$$

where K_P and K_I are the proportional and integral gains of the PI controller, respectively; and ω_c is the angular frequency component regarding positive or negative component in the rotating *dq* frame. The values of ω_c regarding positive and negative sequences are zero and $2\pi \times 120$, respectively.

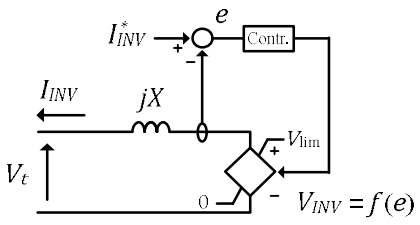

Fig. 3. Simplified model of a PCS-based DER

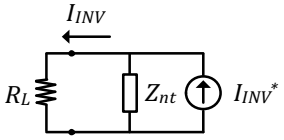

Fig. 4. Current source model

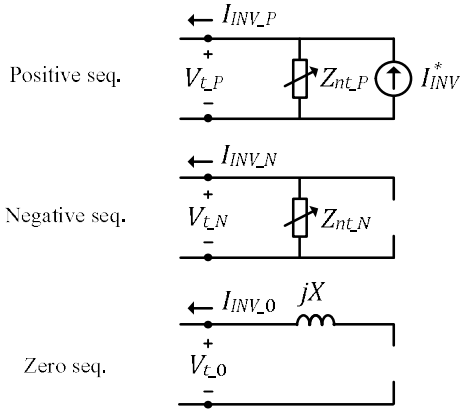

Fig. 5. Positive, negative, and zero sequence parts of the current source model for the fault analysis ($Z_{nt\_P} = \infty$ if the inverter voltage is not limited and $Z_{nt\_N} \neq \infty$)

Here, we note that the Norton impedance varies by the controller gain, load conditions, and sequence components. In particular, the Norton impedance for the positive sequence is infinite ($Z_{nt\_P} = \infty$), which implies that the inverter voltage could increase infinitely. In addition, the zero sequence component of inverter current is generally not controlled; therefore, the respective zero sequence should be modeled from the perspective of a voltage source model. As the DC-link neutral point is not grounded, the zero sequence path of the inverter is open. Accordingly, the current source model for the fault analysis is shown in Fig. 5.

However, it should be noted that this current source model does not include the effect of the inverter voltage limit in (9); thus, the analysis results obtained by this model might be misleading, especially for the case in which the terminal voltage greatly increases.

3. Proposed Method to Derive DER's Static Model

For a proper fault analysis that includes the application of the inverter characteristics of the current control, including the effect of the voltage limit, we need to derive the static voltage source model of a DER that has positive and negative components varying according to the conditions of the distribution grid, as represented in Fig. 6. For this, we solve an optimization problem that has the constraints by the operating limits of the DERs and the grid conditions.

In the first subsection, the constraints for the single-line fault condition are derived in a matrix form. In the second subsection, an optimization problem representing the characteristics of the current control with the constraints is constructed. In the third subsection, the flow of the proposed method is presented. The flow includes a

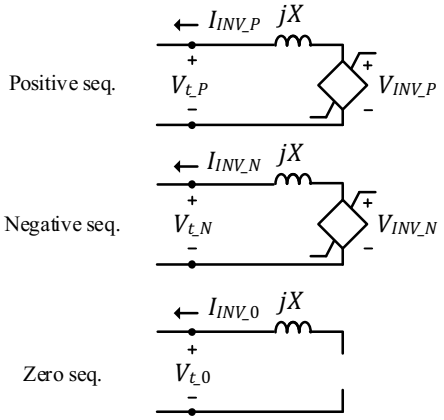

Fig. 6. Positive, negative, and zero sequence parts of the variable voltage source model for the fault analysis

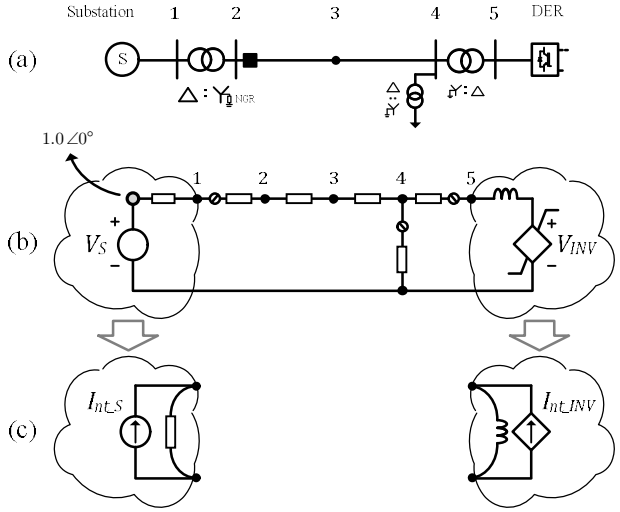

Fig. 7. Distribution grid with 1 DER: (a) single-line diagram; (b) positive sequence part, and (c) corresponding current source models transformed with the Norton theorem

repetitive process to derive a proper current reference to achieve a unity power factor at the DER terminal.

3.1 Constraints for the single-line fault condition

For the fault analysis, the networks for the positive, negative, and zero sequences are separately expressed. Regarding the DER, sources exist in both the positive and negative sequence networks, and we need to derive the equivalent voltage sources for the fault analysis.

Let us assume that there is a distribution grid, and n DERs are interconnected to the grid, where a substation is located at bus 1, and the i^{th} DER is connected to bus m_i. In the grid, a fault occurs at bus r. For simplicity, let us consider only 1 DER, as illustrated in Fig. 7; in this case, $n = 1$, $i = 1$, $m_1 = 5$, and $r = 3$.

First, we obtain the network admittance matrix for the

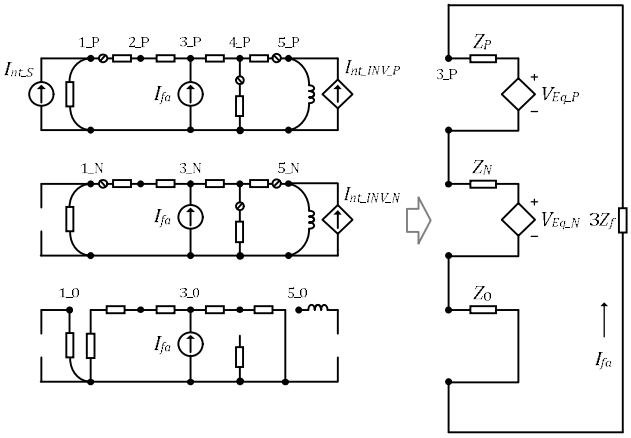

Fig. 8. Positive, negative, and zero sequence parts of the distribution grid shown in Fig. 7 (a) with a single-line fault at bus 3

positive sequence. Note that the voltage sources with internal impedances in series are transformed into current sources with impedances in parallel by the Norton theorem. In addition, note that there no currents are injected into the buses, except for the buses where the sources are connected. Then, the order of the buses is rearranged with a permutation matrix:

$$I_P = Y_P V_P, \tag{11}$$

where $I_P = \begin{pmatrix} I_{1,2,3\_P} \\ 0 \end{pmatrix}$, $Y_P = \begin{pmatrix} Y_a & Y_b \\ Y_c & Y_d \end{pmatrix}$, and $V_P = \begin{pmatrix} V_{1,3,5\_P} \\ V_{2,4\_P} \end{pmatrix}$.

Here, it is noted that the vectors for bus 1, the fault bus (bus 3), and the bus to which the DER is connected (bus 5) are in the 1st, 2nd, and 3rd columns in order. Using the network reduction method [17], the voltage equation of the reduced network with buses 1, 3, and 5 is expressed as

$$V_{R\_P} = Z_{R\_P} I_{R\_P}, \tag{12}$$

where

$V_{R\_P} = V_{1,3,5\_P}$, $I_{R\_P} = I_{1,3,5\_P} = (I_{nt\_S} \quad 0 \quad I_{nt\_INV})^T$,
$Z_{R\_P} = Y_{R\_P}^{-1}$, and $Y_{R\_P} = Y_a - Y_b Y_d^{-1} Y_c$.

The current injected into bus 3 is zero in the normal condition. By substituting the corresponding values into (12), we have the Thevenin equivalent voltage at bus 3 : $V_{Eq\_P} = V_{3\_P}$. In addition, we have the Thevenin impedance seen at bus 3, which is the element at the 2nd row and 2nd column of the matrix Z_{R_P} ($Z_{R\_P,22}$). This is equal to the positive sequence's equivalent impedance Z_P.

Second, in the same way, we calculate the negative sequence's equivalent voltage V_{Eq_N} and impedance Z_N from the respective impedance matrix Z_{R_N}, and the zero sequence's equivalent impedance Z_0 from the respective impedance matrix Z_{R_0}.

Third, after obtaining all of the equivalent impedances,

the fault current is calculated by

$$I_{fa} = (V_{Eq\_P} + V_{Eq\_N})/(Z_P + Z_N + Z_0 + 3Z_f). \quad (13)$$

It is noted that one-third of the fault current I_{fa} is injected into bus 3 when a fault occurs, i.e., $I_3 = I_{fa}$.

By using (12) and (13), the positive, negative, and zero sequence components of the voltages at the buses for the fault condition can be calculated. Once the sequence components are obtained, they are transformed into three phase components (based on the ground) using [18]

$$F_{abc} = AF_{PN0}. \quad (14)$$

3.2 Complex optimization problem

According to the characteristics of the DER and grid in the normal and fault conditions, we construct a convex optimization problem with complex variables:

$$\text{Minimize} \quad \sum_{i=1}^{n} s_i, \quad (15)$$

$$\text{Subject to} \quad s_i \geq \left|I^*_{INVi} - I_{INVi\_P}\right| + \alpha\left|I_{INVi\_N}\right|, \quad (16)$$

where the subscript i signifies the DER number. The summed error between the references and sequence components of the currents of n inverter systems is minimized with (15) and (16). Minimizing the error is the same as the way of the current control working. As noted in (10), the integral gain effect for the negative sequence component is much smaller than that of the positive sequence component. This effect is applied by using the weight α, which is chosen to be 0.001 in this work.

The other constraints to be satisfied are listed in (17)-(27). The positive and negative sequence components of the equivalent voltage seen at bus r in the normal condition are

$$V_{Eq\_P} == Z_{R\_P,2} I_{R\_P}, \quad (17)$$

$$V_{Eq\_N} == Z_{R\_N,2} I_{R\_N}, \quad (18)$$

where

$$I_{R\_P} = (I_{nt\_S} \quad 0 \quad I_{nt\_INV1\_P} \quad \cdots \quad I_{nt\_INVn\_P})^T,$$
$$I_{R\_N} = (0 \quad 0 \quad I_{nt\_INV1\_N} \quad \cdots \quad I_{nt\_INVn\_N})^T.$$

The double equal sign "==" signifies the equality constraints. $Z_{R\_PN,2}$ denotes the second raw component of the matrix Z_{R_PN}. From (13), the constraint for a fault current is

$$I_{fa} == (V_{Eq\_P} + V_{Eq\_N})/(Z_P + Z_N + Z_0 + 3Z_f). \quad (19)$$

The positive and negative sequence components of the i^{th} inverter current have the relations of

$$I_{INVi\_P} == \frac{(V_{INVi\_P} - V_{ti\_P})}{jX}, \quad (20)$$

$$I_{INVi\_N} == \frac{(V_{INVi\_N} - V_{ti\_N})}{jX}. \quad (21)$$

For the positive and negative sequence components of the i^{th} inverter voltage,

$$V_{INVi\_P} == jXI_{nt\_INVi\_P}, \quad (22)$$

$$V_{INVi\_N} == jXI_{nt\_INVi\_N}. \quad (23)$$

It is recalled that, when the neutral point of the DC-link voltage is not grounded, $I_{INVi\_0} = 0$, and V_{INVi_0} is floating (unknown). The positive, negative, and zero sequence components of the terminal voltage of the i^{th} DER have the relations of

$$V_{ti\_P} == Z_{R\_P,i+2} I^f_{R\_P}, \quad (24)$$

$$V_{ti\_N} == Z_{R\_N,i+2} I^f_{R\_N}, \quad (25)$$

$$V_{ti\_0} == Z_{R\_0,i+2} I^f_{R\_0}, \quad (26)$$

where

$$I^f_{R\_P} = (I_{nt\_S} \quad I_{fa} \quad I_{nt\_INV1\_P} \quad \cdots \quad I_{nt\_INVn\_P})^T,$$
$$I^f_{R\_N} = (0 \quad I_{fa} \quad I_{nt\_INV1\_N} \quad \cdots \quad I_{nt\_INVn\_N})^T,$$
$$I^f_{R\_0} = (0 \quad I_{fa} \quad 0 \quad \cdots \quad 0)^T,$$

where $Z_{R\_PN0,i+2}$ denotes the $(i+2)^{\text{th}}$ raw component of the matrix Z_{R_PN0}. Most importantly, from (9), the inverter voltage is limited by

$$\left|V_{INVi\_P}\right| + \left|V_{INVi\_N}\right| \leq \mathrm{V}_{\mathrm{lim}i}. \quad (27)$$

This optimization problem is solved with a convex programming solver [19].

3.3 Procedure of proposed method

In this subsection, a method for obtaining an accurate solution of the fault problem by finding a proper current reference with a repetitive process is presented. The flowchart of the process is shown in Fig. 9.

3.3.1 With a main source (Grid-tied mode)

When DERs are interconnected to the grid, we assume that a unity power factor is achieved with respect to the positive sequence components in both the normal and fault conditions. For this, we need to adjust the references of the inverter currents, which have the same angles as those at the terminal voltages of the DERs, as stated below.

1) Choose the magnitude of the reference $|I^*_{INVi}|$ for the i^{th} DER. The initial angle of the reference is zero ($\theta^1_{Ii} = 0$).
2) Solve the complex optimization problem.
3) Using the solution, calculate a) the difference between

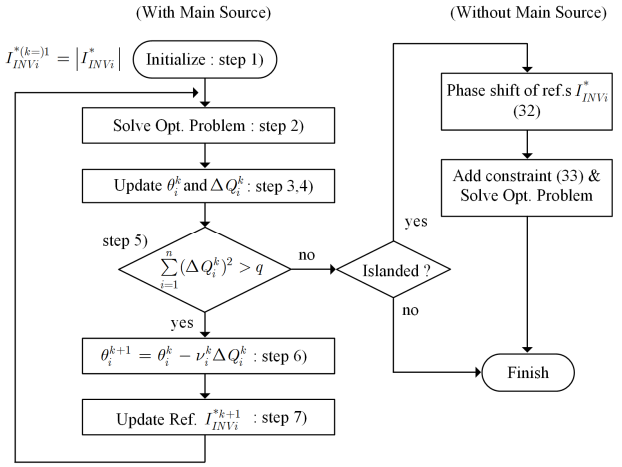

Fig. 9. Flowchart of the proposed method

the angles of V_{ti_P} and I_{INVi_P} and b) the reactive power at the DER terminal as

$$\theta_i^k = \theta_{Vi}^k - \theta_{Ii}^k, \tag{28}$$

where $\theta_{Vi}^k = \tan^{-1}\left(\frac{V_{ti\_Pq}^k}{V_{ti\_Pd}^k}\right)$, $\theta_{Ii}^k = \tan^{-1}\left(\frac{I_{INVi\_Pq}^k}{I_{INVi\_Pd}^k}\right)$, and

$$Q_i^k = \left|V_{ti\_P}^k\right|\left|I_{INVi\_P}^k\right|\sin\theta_i^k. \tag{29}$$

4) Calculate $\Delta Q_i^k = Q_i^k - Q_i^*$, where $Q_i^* = 0$ for a unity power factor.
5) Stop if the squared sum of ΔQ_i^k is less than a predetermined value. Otherwise, proceed to the next step.
6) Update the angle difference θ_i as

$$\theta_i^{k+1} = \theta_i^k - \nu_i^k \Delta Q_i^k, \tag{30}$$

where $\nu_i^k = \left|V_{ti\_P}^k\right|\left|I_{INVi\_P}^k\right|\cos\theta_i^k$. For stable convergence, $\nu_i^k \Delta Q_i^k$ is properly limited.
7) Update the reference I_{INVi}^* and go to 2):

$$I_{INVi}^{*k+1} = |I_{INVi}^*|(\cos\theta_{Ii}^{k+1} + j\sin\theta_{Ii}^{k+1}). \tag{31}$$

3.3.2 Without a main source (Islanded mode)

When the main source is disconnected by the opening of a circuit breaker (for instance, that at bus 2 in Fig. 7) and the DERs are running islanded, a unity power factor cannot be achieved because the power factors at the DER terminals depend on loads that remain in the grid. As matter of fact, in this case, the frequency of the inverter voltage might greatly change owing to the effect of the PLL control, and the DER will be disconnected from the gird by its anti-islanding system in most cases. However, in this work, we will consider the case in which the DER remains connected to the grid without a main source. We assume that the DER has a properly designed PLL system, of which the control output is properly limited; thus, the frequency remains around 60 Hz.

In addition, as the main source to be referenced with the power angle of zero is no longer present, we need to choose a DER as an alternative reference unit. For this, the phases of the inverter current references are shifted on the basis of that of the 1st DER as

$$I_{INVi}^{*\prime} = I_{INVi}^* e^{-j\theta_{\text{sft}}} \quad \text{where} \quad \theta_{\text{sft}} = \tan^{-1}\left(\frac{I_{INV1q}^*}{I_{INV1d}^*}\right). \tag{32}$$

In addition, the following constraint is added to the optimization problem:

$$I_{INV1\_Pq} == 0. \tag{33}$$

Then, the angle of the inverter current of the 1st DER and the respective reference are set to zero, and the bus voltages and currents will be represented on the basis of the angle.

4. Simulation Results

To verify the validity of the proposed method, computer simulations are carried out, where the results of the proposed method are compared with those obtained from dynamic simulations using MATLAB Simulink. The model of a DER for Simulink was constructed as shown in Fig. 1 and 2. The rated power of a DER is 10 MW, and its inverter system consists of 10 identical 1 MW inverters. The parameters of the 1 MW inverter used for the Simulink simulation are listed in the Appendix.

The configuration of the distribution grid for the simulation is shown in Fig. 10, and the impedances are

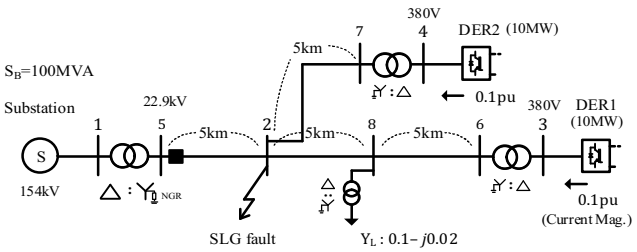

Fig. 10. Configuration for the simulation

Table 1. Impedances per-unit

	Positive, Negative	Zero
substation (s/s) int. impedance	$j0.01$	$j0.01$
s/s tr. impedance (bus 1-5)	$j0.34$	$j0.49$
DER's int. impedance (filter $-jX$)	$j13.5$	$j13.5$
DER's tr. impedance (bus 3-6 and 4-7)	$j0.60$	$j0.60$
line impedances (bus 5-2, 7-2, 8-2, 6-8)	$0.1749 + j0.3876$	$0.45 + j1.14$

Table 2. Sequence components of the bus voltages (case 1)

Bus No.	Comp.	Simulink (60 Hz)		Proposed (60 Hz)	
		Mag.(pu)	Ang.(deg.)	Mag.(pu)	Ang.(deg.)
1	Pos.	0.9952	-0.03	0.9952	-0.02
	Neg.	0.0044	-101.31	0.0044	-102.36
	Zero	0.0	-	0.0	-
2 (SLG)	Pos.	0.6445	34.07	0.6416	35.05
	Neg.	0.3314	-144.62	0.3335	-145.70
	Zero	0.3052	-142.70	0.3081	-144.14
3 (DER1's terminal)	Pos.	0.6467	14.44	0.6464	15.63
	Neg.	0.3246	-116.90	0.3251	-117.67
	Zero	-	-	-	-
4 (DER2's terminal)	Pos.	0.6534	12.76	0.6514	13.90
	Neg.	0.3328	-114.83	0.3335	-115.70
	Zero	-	-	-	-
5	Pos.	0.8346	28.80	0.8319	29.10
	Neg.	0.1529	-131.30	0.1540	-132.36
	Zero	0.0884	-127.17	0.0893	-128.71
6	Pos.	0.6502	39.23	0.6491	40.33
	Neg.	0.3236	-146.80	0.3251	-147.67
	Zero	0.0606	-125.34	0.0613	-126.79
7	Pos.	0.6565	37.60	0.6542	38.64
	Neg.	0.3317	-144.73	0.3335	-145.70
	Zero	0.1018	-128.20	0.1029	-129.64
8 (Load)	Pos.	0.6384	35.66	0.6365	36.71
	Neg.	0.3233	-149.69	0.3251	-147.67
	Zero	0.1818	-139.85	0.1835	-141.29

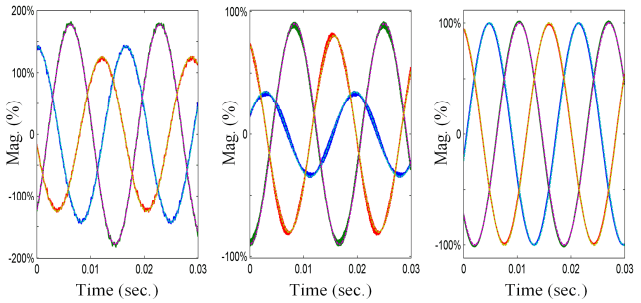

Fig. 11 Comparison of the results of obtained by the Simulink simulation and proposed method in case 1: (a) inverter line voltages; (b) terminal line voltages, and (c) inverter currents of DER1

listed in Table 1. The base power is 100 MVA. DERs are operated at their rated power with a unity power factor at the terminal buses before the transformers for grid integration. In this work, the maximum current of a DER in (7) is set to be equal the rated value (0.1 pu). The terminal bus line voltage of the DERs is 380 Vrms. Further, a load is connected to bus 8 through a D-Yg transformer.

First, we consider the case in which a single line ground (SLG) fault occurs at bus 2 and the circuit breaker (CB) at bus 5 is closed so that the main source is still active (case 1). Fig. 11 shows a comparison of waveforms obtained from the Simulink simulation (solid line) and those generated on the basis of the results of the proposed method (dotted line). Fig. 11 (a), (b), and (c) show the

Table 3. Sequence components of the currents (case 1)

Bus No.		Comp.	Simulink (60 Hz)		Proposed (60 Hz)	
From	To		Mag.(pu)	Ang.(deg.)	Mag.(pu)	Ang.(deg.)
5	2	Pos.	0.4749	-54.18	0.4819	-55.55
		Neg.	0.4374	-41.13	0.4399	-42.36
		3Zero	0.5421	-37.14	0.5467	-38.71
7	2	Pos.	0.0998	43.41	0.1000	43.88
		Neg.	0.0015	84.26	0.0	-
		3Zero	0.5100	-38.07	0.5144	-39.64
8	2	Pos.	0.0453	76.96	0.0450	75.41
		Neg.	0.0340	24.04	0.0332	21.02
		3Zero	0.3038	-35.22	0.3064	-36.79
6	8	Pos.	0.0998	45.41	0.1000	45.59
		Neg.	0.0015	82.23	0.0	-
		3Zero	0.3038	-35.22	0.3064	-36.79
DER1	3	Pos.	0.0999	15.32	0.1000	15.59
		Neg.	0.0015	116.14	0.0	-
		3Zero	0.0	-	0.0	-
DER2	4	Pos.	0.0999	13.33	0.1000	13.88
		Neg.	0.0015	118.20	0.0	-
		3Zero	0.0	-	0.0	-

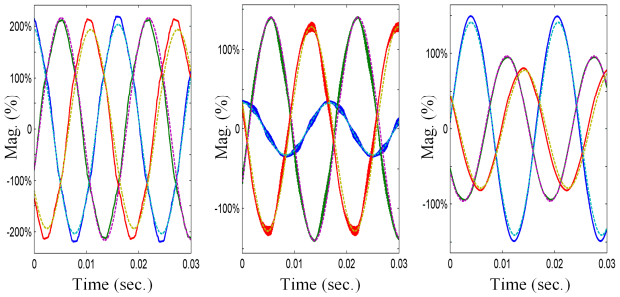

Fig. 12. Comparison of the results of the Simulink simulation (60.5 Hz) and proposed method (60 Hz) in case 2: (a) inverter line voltages, (b) terminal line voltages, and (c) inverter currents of DER1

inverter line voltages, terminal line voltages, and inverter currents of DER1. The inverter voltage waveforms obtained with the Simulink simulation are actually pulses; thus, they are filtered with a 1st-order low-pass filter with a cut-off frequency is 9 kHz. As seen in the figure, the results obtained by the proposed method exactly match those of the Simulink simulation. In addition, the positive, negative, and zero sequence components are calculated using a signal processing technique on the basis of the waveforms obtained from the Simulink simulation and are listed with those of the proposed method in Table 2 and 3. It is noted that the angles of the positive sequence components of the terminal voltages and currents of the DERs are almost the same for the results obtained by both methods, which implies that a unity power factor is achieved

Second, we consider another case in which the CB at bus 5 is opened after an SLG fault; thus, there is no main source, but the DERs are still running and islanded (case 2). It is assumed that the frequencies of both of the inverter

Table 4. Sequence components of the bus voltages (case 2)

Bus No.	Comp.	Simulink (60.5 Hz)		Proposed (60 Hz)	
		Mag.(pu)	Ang.(deg.)	Mag.(pu)	Ang.(deg.)
2 (SLG)	Pos.	0.8351	69.89	0.8307	66.85
	Neg.	0.6864	-112.53	0.6967	-117.14
	Zero	0.1499	-96.30	0.1441	-93.49
3 (DER1's terminal)	Pos.	0.9323	43.26	0.9214	40.55
	Neg.	0.6034	-83.31	0.6213	-88.81
	Zero	–	–	–	–
4 (DER2's terminal)	Pos.	0.9191	43.65	0.9084	41.04
	Neg.	0.6366	-82.00	0.6524	-87.17
	Zero	–	–	–	–
6	Pos.	0.8907	70.39	0.8836	67.59
	Neg.	0.6316	-113.20	0.6456	-118.38
	Zero	0.0298	-78.94	0.0287	-76.13
7	Pos.	0.8748	70.96	0.8688	68.13
	Neg.	0.6664	-111.88	0.6785	-116.76
	Zero	0.0500	-81.86	0.0481	-78.99
8 (Load)	Pos.	0.8518	69.15	0.8463	66.24
	Neg.	0.6506	-113.86	0.6626	-118.74
	Zero	0.0893	-93.47	0.0858	-90.63

Table 5. Sequence components of the currents (case 2)

Bus No.		Comp.	Simulink (60.5Hz)		Proposed (60Hz)	
From	To		Mag.(pu)	Ang.(deg.)	Mag.(pu)	Ang.(deg.)
7	2	Pos.	0.1004	26.43	0.1000	28.30
		Neg.	0.0502	-19.18	0.0441	-16.57
		3Zero	0.2490	8.18	0.2406	11.01
8	2	Pos.	0.0469	-29.74	0.0424	-29.14
		Neg.	0.0915	24.34	0.0916	25.43
		3Zero	0.1485	11.01	0.1434	13.87
6	8	Pos.	0.1013	29.99	0.1000	30.00
		Neg.	0.0476	-20.65	0.0412	-17.51
		3Zero	0.1485	11.01	0.1434	13.87
DER1	3	Pos.	0.1016	-0.01	0.1000	0.0
		Neg.	0.0475	9.21	0.0412	12.45
		3Zero	0.0	–	0.0	–
DER2	4	Pos.	0.1007	-3.56	0.1000	-1.70
		Neg.	0.0501	10.69	0.0441	13.43
		3Zero	0.0	–	0.0	–

Table 6. Magnitudes of the SLG fault current and bus-8 B-phase voltage

Case	Load level	Simulink		Proposed	
		Fault cur.	B8 b-ph vol.	Fault cur.	B8 b-ph vol.
Grid-tied (case 1)	L1	1.3544	0.9426	1.3649	0.9435
	L2	1.3615	0.9348	1.3666	0.9350
	L3	1.3631	0.9228	1.3672	0.9242
Islanded (case 2)	L1	0.4283	1.8071	0.4246	1.8451
	L2	0.4095	1.5980	0.4175	1.6457
	L3	0.3974	1.3612	0.3837	1.3849

voltages of the DERs remain around 60 Hz. In the Simulink simulation, the PLL control output is properly limited; thus, the frequency does not exceed 60.5 Hz. Fig. 12 shows a comparison of the results, similar to Fig. 11. It is seen that some harmonic components are included in the waveforms obtained with the Simulink simulation. These waveforms are slightly different than those of the proposed method because the frequency has a difference of 0.5 Hz owing to the effects of the PLL control and current control. Table 4 and 5 list the positive, negative, and zero sequence components obtained with the Simulink simulation and proposed method. The values are slightly different, but they are almost the same in magnitude and phase.

In addition, the magnitudes of the fault currents and bus voltage obtained by the proposed method and Simulink simulations are compared. The bus-8 B-phase voltage, which has the largest magnitude among the three phase components, is chosen for comparison. Table 6 summarizes the results for the two cases under three different load conditions: (L1) no load, (L2) a 5 MW and 1 MVar (inductive) load (Y_L : $0.05 - j0.01$), and (L3) a 10 MW and 2 MVar load (Y_L : $0.10 - j0.02$). The current and voltage according to load level for the results obtained by both methods change with the same tendency. These simulation results confirm that the proposed method works very well in cases where the DERs are grid-tied or islanded.

5. Discussion

As mentioned over the paper, a PCS-based DER is considered as a current source unlike the conventional distributed power sources considered as a voltage source. However, recalling that the current control is performed by varying the inverter voltage, in some fault conditions such the magnitude of voltage at the DER's integration point increasing too large, it is evident that the magnitude of the inverter voltage should be larger. This does not happen because the inverter voltage cannot exceed their limits, and, in consequence, the inverter current control fails. In addition, as the DER is usually operated in unity power factor, the angles of the current source and the voltage at the integration point should be matched. To include these factors into the modeling, it was necessary to apply iterative processes with optimization techniques as well as symmetrical analysis methods.

In power grid, steady state analysis is often very important. For instance, many transient voltage surge suppressors are installed in power grid to let sudden surplus energy flowing into the ground so that power equipment is protected from the voltage surge. These suppressors are not designed to run against high voltage in steady state. For this case, the proposed can be applied to check if effective grounding is satisfied when fault happened and to choose proper surge suppressors and their settings.

Lastly, it is stressed that the proposed method is designed for steady state analysis related to fundamental frequency, and thus it would not be adequate for analysis related to transient characteristics. In addition, as this work is verified by computer simulations, we expect that results might be slightly different by factors such as harmonics not considered in the simulations.

6. Conclusions

In this work, we proposed a fault analysis method using an optimization problem in which the constraints are derived according to the DER characteristics and grid conditions. While the method with a current source model for a DER only works for the condition with a main source, the proposed method is useful with and without a main source. In addition, as the proposed method produces the information of inverter voltages in fault conditions, it is expected to be beneficial in analyzing the fault effect by the inverter voltage limit. The usefulness of the proposed method is demonstrated with computer simulations. This work is expected to be useful for the steady-state fault analysis of a power distribution grid with multiple PCS-based DERs.

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Dong-Eok Kim received the B.S. and M.S. degrees in electrical engineering from Yeungnam University, Gyeongbuk, Korea, in 2005 and 2008, respectively, and the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2014. Currently, he is a Senior Researcher at KEPCO Research Institute, Daejeon, Korea. His research interests include power system modeling, dynamics, and fault analysis, as well as control of power systems.

Namhun Cho received the B.S. and M.S. degrees in electrical engineering from Chung-Ang University, Seoul, Korea, and Chungnam National University, Daejeon, Korea, in 1992 and 2002, respectively, and the Ph.D. degree in electrical and computer engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2013. He joined Korea Electric Power Corporation in 1992 and he is currently a Principle Researcher at KEPCO Research Institute, Daejeon, Korea.

Appendix

Table 7. Parameters for the MATLAB Simulink simulation

		Parameters
DC/AC PWM Converter (Inverter for grid integration)		▪ LCL filters - (inv. side) $R_{f1} = 0.001\ \Omega,\ L_{f1} = 0.25$ mH - (grid side) $R_{f2} = 0.001\ \Omega,\ L_{f2} = 0.25$ mH - (filter cap. side) $C_f = 45\ \mu F,\ R_{fd} = 2\ \Omega$ ▪ DC-link capacitor: $C_{dc} = 30000\ \mu F$ ▪ Sampling frequency: $f_s = 20$ kHz ▪ Switching frequency: $f_{sw} = 10$ kHz
Control	Ref. & limits	▪ DC-link voltage reference: $V_{dc}^{*} = 1060$ V (resistor switch turned-on if $V_{dc} > 1165$ V) ▪ DC-link voltage controller output's limit : $I_{MAX} = 2150A_{peak}$ (1.0 pu) ▪ Current controller output's limit : $V_{INV\_lim} = 530\ V_{peak}$ (1.7 pu) ($V_{INV\_MAX} = 749.5\ V_{peak}$ (2.42 pu)) ▪ Inverter (line) voltage limit in (9) : $V_{lim(ll)} = 1165\ V_{peak}$ (2.167 pu)
	Gains	▪ Voltage controller gains - Proportional gain: $K_{P\_dc} = 2\zeta_{dc}C_{dc}\omega_{dc}$, - Integral gain: $K_{I\_dc} = C_{dc}\omega_{dc}^2$ ($\zeta_{dc} = 1,\ \omega_{dc} = 200$) - Anti-windup gain: $K = 1/K_{p\_dc}$ ▪ Current controller gains - Proportional gain: $K_P = 2\zeta_c L\omega_c$, - Integral gain: $K_I = L\omega_c^2$ ($\zeta_c = 0.707,\ L = L_{f1} + L_{f2},\ \omega_c = 2000$)