An Integrated Compensation Algorithm for PCC Voltage Fluctuation and Unbalance with Variable Limit of Positive and Negative Sequence Currents

Ji-Hoon Im*, Seung-Ho Song† and Sung-Min Cho*

Abstract – This paper proposes a point of common coupling (PCC) voltage compensation algorithm using a current limitation strategy for use in distributed generation (DG). The proposed strategy maintains the PCC voltage by prioritizing currents when an output current reference is larger than the current capacity of the power condition system (PCS) of the DG. With this strategy, the DG outputs the active current, reactive current, and the negative sequence current. The DG uses the reactive current for maintaining the PCC voltage within a normal range; the negative sequence current is used for reducing the PCC voltage unbalance. The proposed method was verified using PSIM simulation and experimental results.

Keywords: Distributed generation, Unbalanced voltage conditions, Dual current control, Positive sequence, Negative sequence, Current limitation

1. Introduction

In recent years, distributed generation (DG) has been regarded as a key alternative to centralized power generation for future electric grid systems. The use of DG is also being promoted due to rising concerns about environmental problems and due to efforts for improving the energy efficiency of power systems [1-4].

However, the integration of DG in power grids is accompanied by a number of electrical challenges such as maintaining power quality and changing established operating strategies of conventional power plants. Studies of these electrical challenges also reveal the presence of voltage variation, due to the outputs of DG systems, at the point of common coupling (PCC) as one of the most common problems of using DG [5-7]. Voltage variations seriously occur when the DG resource is connected to weak grid conditions (e.g., when connected to a small isolated network or when there is a high penetration of DG), and can increase because of the reverse power flow of DG. In the worst case, an ineffective power control of DG may result to the loss of voltage stability in the power grid [8]. According to the standard, IEEE 1547.2-2008, the voltage regulation range caused by DG should be limited to 5% only for connections to a low voltage grid [9].

In maintaining voltage stability, the unbalanced voltage conditions must be considered at the PCC. The unbalanced voltage conditions may worsen the voltage variation because the voltage peak under unbalanced voltage conditions is larger than the case under balanced voltage conditions.

This paper describes a method for solving the voltage variation problem by using DG only. By using current injection, the purpose of the method is not only to suppress the voltage variation but also to reduce the unbalanced voltage conditions.

Traditionally, devices with a reactive power source are used to maintain the balance of voltage profile. One conventional method that uses reactive power for voltage control is by installing capacitor banks. However, it is difficult to get the linear compensation of the reactive power with this method, and redesigning of the capacitor banks is required when the new DG is installed or the power grid is changed (e.g., change in loads, by the utility, etc.) [10].

A static synchronous compensator (STATCOM) is more efficient in injecting reactive power, especially STATCOM with DG (also known as, "D-STATCOM") [11, 12]. STATCOM has a faster response and a softer effect on transient errors than when a capacitor bank is used. Therefore, the voltage profile control can maintain the voltage of PCC more precisely. But, since this method uses a PI controller to maintain the voltage at PCC, connecting a lot of STATCOMs may lower the voltage stability of the grid. This method may be more expensive because the STATCOM will be an added device to the DG system.

If a DG system can compensate its own PCC voltage, using additional devices that compensate voltage variations will no longer be necessary. Proposed in [13, 14] is the use of the power conversion system (PCS) of the DG to meet the required amount of reactive power and to compensate the voltage variation. The magnitude of the PCC voltage

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variation is calculated using the equivalent circuit parameters and the output power of the DG. In addition, this assumes that the reactive power controller knows the active power outputs. Finally, it is possible to maintain the voltage profile at the PCC without a PI controller by using information: circuit parameters and DG active power.

The aforementioned methods are based on reactive power compensation for the reduction of voltage variation. However, even if these voltage compensation methods are implemented, the maximum or minimum voltage may still exceed the stable voltage range if a PCC voltage unbalance exists. In this paper, a new algorithm, which can effectively reduce the voltage variation due to the DG output even during an unbalanced grid fault, is proposed for a DG systems controller. And since the proposed method requires an increased amount of current, a method for prioritizing and limiting the currents using a step-by-step process is also proposed to solve the capacity problem of DG.

2. Current Vector with Positive Sequence Current and Negative Sequence Current

2.1 Voltage vector and current vector

If the traditional DG system which only outputs the active power is simplified into a current source with a phase locked loop (PLL), the current vector angle of the DG can be assumed to be the same as that of the voltage vector. However, the DG can be independent from the vector angle of the voltage because a DG with an inverter can be used for 4-quadrant operation. Furthermore, if the output current of the DG includes the negative sequence, the angular speed will be also different from that of the voltage vector through the PLL.

To help understand this theory, a vector diagram is shown in Fig. 1, which shows the voltage vector with PLL and the currents that include the active power only. In Fig. 1(a), the voltage vector with magnitude, V_p, aligned with q-axis in synchronous frame, is expressed with a counter-clockwise rotation sequence and an initial angle, θ_p. Fig. 1(b) shows the positive sequence q-axis current with the same angle as the voltage. Fig. 1(c) shows a synthesized current vector, I_p.

If the currents include the negative sequence, the current vector cannot be expressed with same synchronous frame. Fig. 2 shows the current vector with negative sequence. The negative sequence current vector (in Fig. 2(a)) with magnitude of I_n, meanwhile, is expressed with a clockwise rotation sequence with another initial angle against the positive sequence. To express all components in one vector diagram, a dq-stationary frame is used. Fig. 2(b) shows the synthesized current vector with all components from (1), (2) and (3). The current vector locus is the sum of the all components that seems to trace an elliptical orbit and, as a result, does not have a constant angular speed.
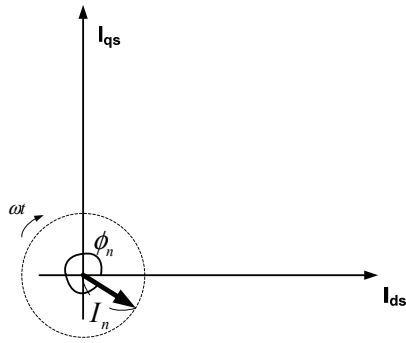
(a)

(b)

(c)
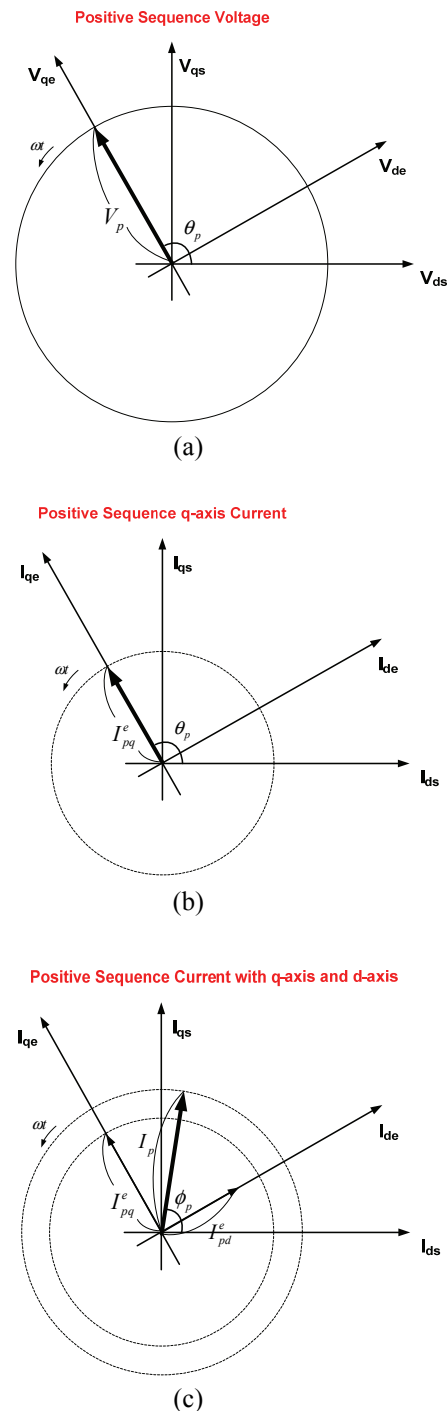
Fig. 1. The voltage vector and the current vector with grid connection: (a) The voltage vector with synchronous frame; (b) The q-axis current vector from the voltage vector axis; (c) The current vector including reactive current

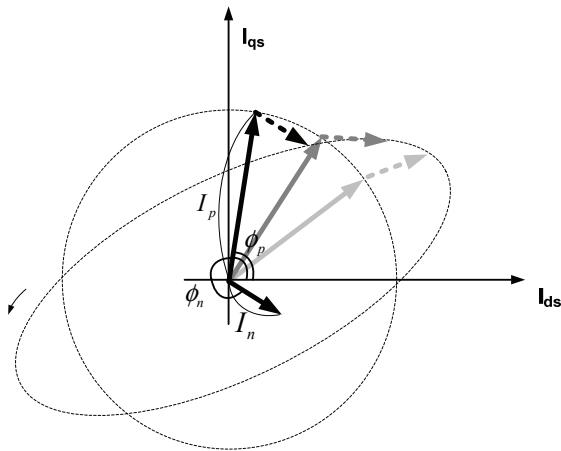$$i(t) = I_p e^{j(\omega t + \phi_p)} + I_n e^{-j(\omega t + \phi_n)} \qquad (1)$$

$$I_p = \sqrt{\left(I_{pde}\right)^2 + \left(I_{pqe}\right)^2} \qquad (2)$$

Negative Sequence Current

(a)

Synthesized Current Vector Locus

(b)

Fig. 2. The current vector with negative sequence: (a) a negative sequenced current vector with stationary frame; (b) a synthesized current vector trajectory

$$I_n = \sqrt{\left(I_{nde}\right)^2 + \left(I_{nqe}\right)^2} \tag{3}$$

$$I_{max} = I_p + I_n \tag{4}$$

$$\omega t = \frac{\phi_p + \phi_n}{2}, \quad \frac{\phi_p + \phi_n}{2} + \pi \tag{5}$$

2.2 Current limitation

As shown in Fig. 2, the current vector trajectory is elliptical in shape. The maximum current vector is the sum of the amplitude of the positive sequence current and that of the negative sequence current, as shown in (4). The angle of the maximum current vector is shown in (5).

The current capacity of the inverter is limited by some devices (e.g., a power electronic switch, etc.). Assuming that the PCC voltage is regulated, the current capacity vector trajectory will be circular in shape. Fig. 3 shows a current limitation within inverter current capacity, and if the current vector is limited, some issues may arise: first, it
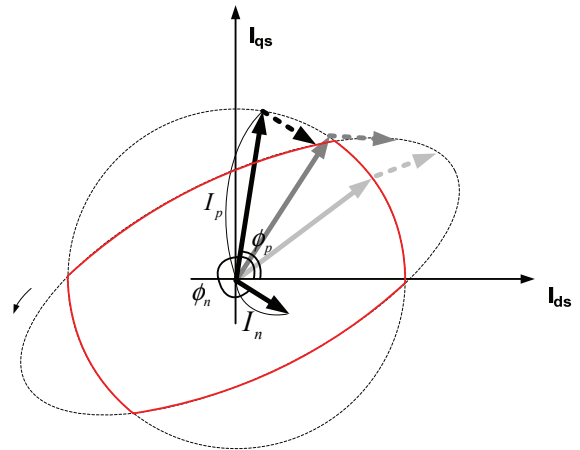
Traditional Current Limitation

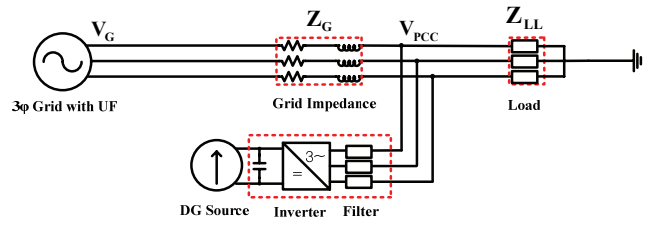**Fig. 3.** A current limitation within inverter current capacity

Fig. 4. T-equivalent circuit model

is difficult to control the ratio between the positive sequence current and the negative sequence current; second, the output current may include high harmonic distortion.

3. Proposed Voltage Compensation under Unbalanced Voltage Conditions

3.1 Analysis of PCC voltage variation

Regardless of the complexity of the actual power system network, the equivalent T-shaped circuit diagram, as shown in Fig. 4, can be derived at the PCC for simple calculations. If the DG system is simplified into a current source with PLL, the voltage variation at the PCC will be related to the output current of the DG and the equivalent impedance at the PCC, as shown in (6).

$$\mathbf{V}_{PCC} = \mathbf{V}_{PCC0} + \mathbf{Z}_{effect}\mathbf{I}_{DG} \tag{6}$$

Where $\mathbf{V}_{PCC}$ is the PCC voltage complex vector with DG output current; $\mathbf{V}_{PCC0}$ is the PCC voltage complex vector without DG output current; $\mathbf{I}_{DG}$ is the DG output current complex vector; and $\mathbf{Z}_{effect}$ is the equivalent impedance complex vector, including amplitude and the angle at PCC. $\mathbf{Z}_{effect}$ is calculated by using $\mathbf{Z}_{G}$ and $\mathbf{Z}_{LL}$ [14].

3.2 Positive sequence compensation current calculation

The positive sequence voltage variation at the PCC is related to the positive sequence output current of the DG. The positive sequence current is divided into two orthogonal current vectors: the q-axis and the d-axis current vectors. If the DG outputs only the active current with the same phase angle as the voltage vector, from (6), the new voltage vector at PCC, $\mathbf{E}_{\mathbf{P\_new}}$, can be drawn as shown in Fig. 5(a). As a result, the amount of voltage variation can be shown by the subtraction of the magnitude of the two voltage vectors, $\mathbf{E}_{\mathbf{P\_new}}$ and $\mathbf{E}_{\mathbf{P0}}$.

To reduce the voltage variation due to the output current of the DG, this paper used the reactive current with the right phase angle from the voltage vector. If the amount of reactive current injected is enough to reduce the voltage variation to 0, the magnitude of the final voltage vector, $\mathbf{E}_{\mathbf{P}}$, can be the same as that of the original voltage vector, $\mathbf{E}_{\mathbf{P0}}$. The required value of the reactive current, I_{pde}, can

(a)

(b)
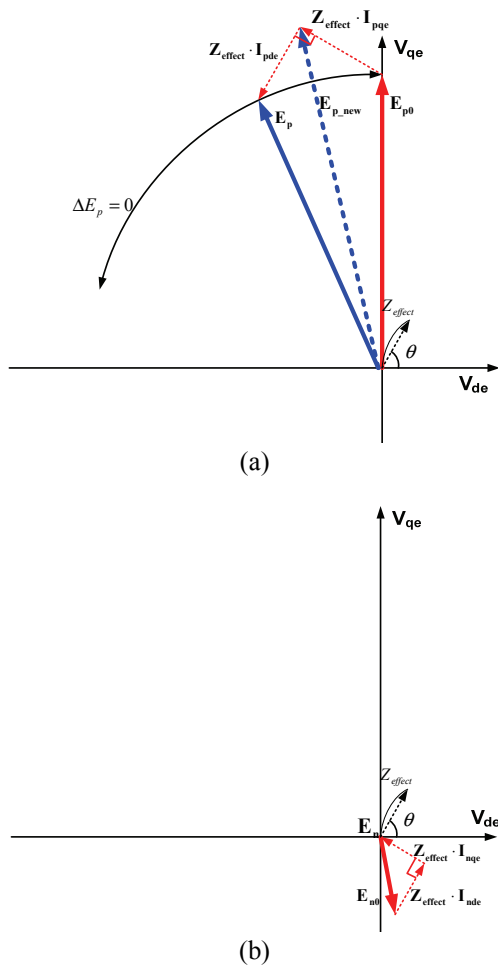
Fig. 5. Proposed current compensation at dq-frame: (a) the positive sequence voltage compensation for $\Delta E_p = 0$; (b) the negative sequence voltage compensation for $E_n=0$

then be obtained from (7),

$$I_{pde} = \frac{(E_{p0}\sin\theta - \sqrt{(E_{p0})^2 - (E_{p0}\cos\theta + Z_{effect}I_{pqe})^2})}{Z_{effect}} \quad (7)$$

Where I_{pqe} is the q-axis positive sequence current of DG; Z_{effect} is the amplitude of the equivalent impedance complex vector at PCC, θ is the phase angle of equivalent impedance complex vector at PCC, and E_{p0} is the magnitude of the positive sequence voltage complex vector without DG output.

3.3 Negative sequence compensation current calculation

To reduce the negative sequence voltage for adjusting unbalanced voltage conditions, this paper uses an injection method of the compensation current, which is composed of a negative sequence current only. The proposed compensation method uses a similar approach that is used in the positive sequence voltage compensation.

The negative sequence voltage vector without compensation current, $\mathbf{E}_{\mathbf{n0}}$, can be reduced by two voltage vectors related with the d-axis and q-axis negative sequence currents shown in Fig. 5(b). From (6), the d-axis and q-axis negative sequence currents, I_{nde} and I_{nqe}, can be used in (8) to reduce the negative sequence voltage to 0.

$$\begin{bmatrix} I_{nde} \\ I_{nqe} \end{bmatrix} = \frac{1}{Z_{effect}} \begin{bmatrix} -\cos\theta & -\sin\theta \\ \sin\theta & -\cos\theta \end{bmatrix} \begin{bmatrix} E_{nde} \\ E_{nqe} \end{bmatrix} \quad (8)$$

Where, E_{nde} and E_{nqe} are the d-axis and q-axis negative sequence voltage at the PCC in the synchronous reference frame with the positive sequence voltage. As a result of this method, the negative sequence current is determined by the negative sequence voltage and the equivalent impedance complex vector.

4. Current Limitation with Priority in a Distributed Generation

The DG is able to supply not only the positive sequence q-axis current and the positive sequence d-axis current, but also the d-axis and q-axis negative sequence currents. However, if the sum of the all required currents is more than the allowable current capacity of the inverter, some types of current may be either limited or uncontrollable. In order to solve this problem, the priority of output currents (also referred to as "current priority" in this paper) must be decided among the active current (the positive sequence q-axis current), the reactive current (the positive sequence d-axis current), and the d-axis and q-axis negative sequence currents.

Here are some rules for setting the current priority.

① Algorithm is for DG
② The positive sequence voltage is liable to variation by DG
③ The negative sequence voltage doesn't change with a general inverter (Only has positive sequence current output)
④ It needs to be considered due to the grid voltage conditions

Within the normal voltage range at the PCC, the active current has higher priority due to its basic duty of supplying the active power. The reactive current then has the second priority because the active current of the DG itself causes the voltage variation; and it is necessary that the DG reduces the voltage variation by maintaining the PCC voltage within the normal voltage range. The rest of the output currents (e.g., the negative sequence currents) are supported by the remaining inverter current capacity.

In case that the reactive current is limited by the active current, the calculated reactive current is expressed in (9). In case that the positive sequence current is less than the allowable current capacity, and the sum of the positive sequence currents and the negative sequence currents exceeds the current limit of the inverter, the d-axis and q-axis negative sequence currents have reduced reference

value as shown in (10) and (11). In this case, the d-axis and q-axis negative sequence currents are both reduced in proportion with the scaling coefficient, K. Fig. 6 shows the flow chart based on this current prioritization process.

$$I_{pde}^* = \sqrt{I_{max}^2 - \left(I_{pqe}^*\right)^2} \tag{9}$$

$$I_{nde}^* = K \cdot I_{nde0}^* = \frac{I_{max} - \left(\sqrt{\left(I_{pde0}^*\right)^2 + \left(I_{pqe0}^*\right)^2}\right)}{\left(\sqrt{\left(I_{nde0}^*\right)^2 + \left(I_{nqe0}^*\right)^2}\right)} I_{nde0}^* \tag{10}$$

$$I_{nqe}^* = K \cdot I_{nqe0}^* = \frac{I_{max} - \left(\sqrt{\left(I_{pde0}^*\right)^2 + \left(I_{pqe0}^*\right)^2}\right)}{\left(\sqrt{\left(I_{nde0}^*\right)^2 + \left(I_{nqe0}^*\right)^2}\right)} I_{nqe0}^* \tag{11}$$

Fig. 7 shows the full block diagram with the "current limitation with priority" block at the grid-side converter (GSC). All currents and voltages of the GSC are separately decomposed into the positive sequence and the negative sequence components [15]. The positive sequence current and the negative sequence current are then added to the conventional control algorithms. Finally, the aforementioned "Current Limitation with Priority" block regenerates the calculated reference values.
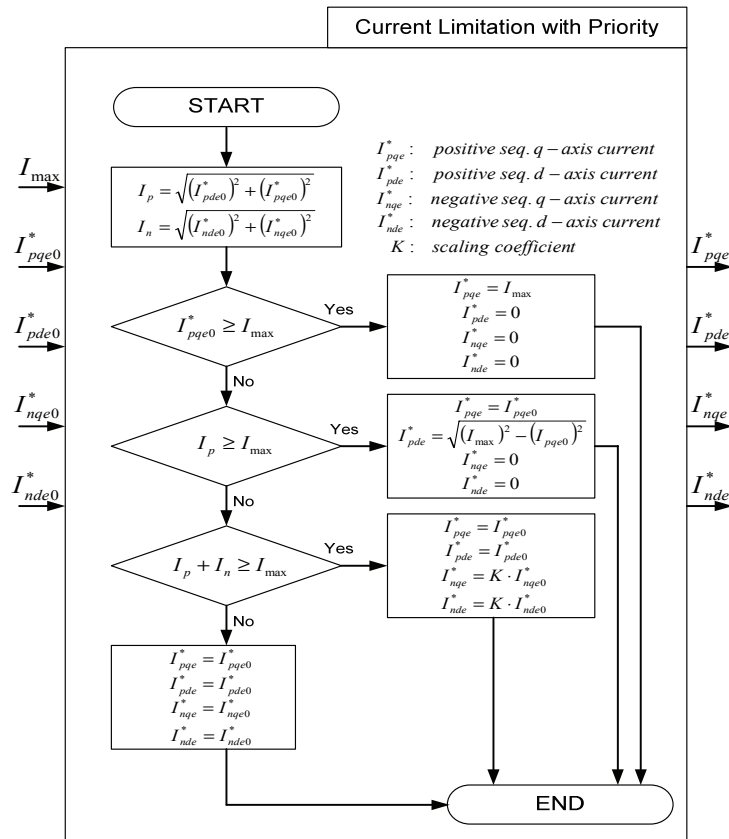

Fig. 6. Whole GSC block diagram with the PCC voltage compensation and the current limitation
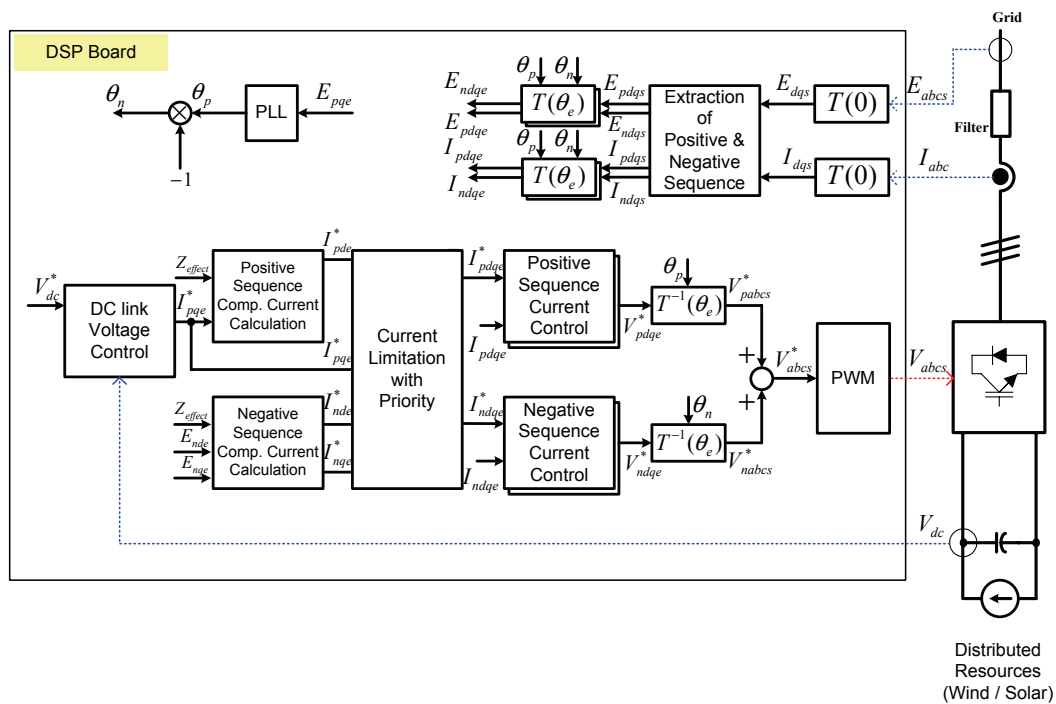
Fig. 7. GSC block diagram with PCC voltage compensation and current limitation

5. Simulation and Experimental Results

5.1 Experimental setup and conditions

The proposed priority algorithm is assessed by means of computer simulations and experimental results. The simulations and experiments were accomplished with a properly developed model, illustrated in Fig. 4. This experimental setup assumes that the grid includes the unbalanced voltage conditions, and that the simplified network system has proper line impedance in order to make sensitive connection point as an injection of currents.

Table 1 lists the network parameters, and the line and load data. The unbalance factor (UF) is defined as the ratio of the negative sequence voltage to the positive sequence voltage [16]. This line impedance means that the short circuit ratio (SCR) is approximately 10 and the X/R ratio is 3 [17]. The rated power of the DG source is assumed to have a value of 3 kW. The inverter is driven by a SVPWM with a switching frequency of 4 kHz.

5.2 Voltage compensation of DG

To verify the feasibility of the proposed dual sequence control scheme, computer simulations and experiments were conducted with the scenarios shown in Table 2. In the simulations, we used a current controller with 100 rad/s bandwidth. Fig. 8 shows the experimental results of the PCC voltage $\{E_a, E_b, E_c\}$, the current of DG $\{I_a, I_b, I_c\}$, the positive sequence voltage of PCC $\{I_p\}$, the negative sequence voltage of PCC $\{I_n\}$, the d-q axis positive

Table 1. The caption must be followed by the table

| Description	Symbol	Value	Unit
Grid Voltage Source	V_G	220	V
Unbalance Factor	UF	3	%
Grid Impedance	Z_G	0.4+j1.17	Ω
Load Impedance	Z_{LL}	20	Ω

Table 2. Voltage variation and compensation scenario when DG's output is variable connected to the unbalance grid

Event	Section	Time	Results
Nothing	1	~0.1 s	None
The q-axis positive sequence current output from 0 pu to 0.5 pu (4A)	2	0.1 s~ 0.2 s	V_P changes from 1 pu (128V) to 1.01 pu (129V)
The q-axis positive sequence current output from 0.5 pu to 1 pu (8A)	3	0.2 s~ 0.3 s	V_P changes from 1.01 pu to 1.02 pu (130V)
The d-axis positive sequence current compensation with equation (2)	4	0.3 s~ 0.4 s	V_P changes from 1.02 pu to 1 pu
Negative sequence current output with equation (4)	5	0.4 s~ 0.5 s	V_n changes from 0.03 pu (4V) to 0 pu (0V)

sequence current commands and responses in the synchronous frame $\{I^*_{pde}, I^*_{pqe}, I_{pde}, I_{pqe}\}$, and the d-q axis negative sequence current commands and responses in the synchronous frame $\{I^*_{nde}, I^*_{nqe}, I_{nde}, I_{nqe}\}$.

For the voltage variation, in Section 2 and Section 3 of Fig. 8 show the responses to the step change in the positive sequence q-axis current commands, beginning from 0 pu to 0.5 pu (4A)and 1 pu (8A). In the simulation results of these
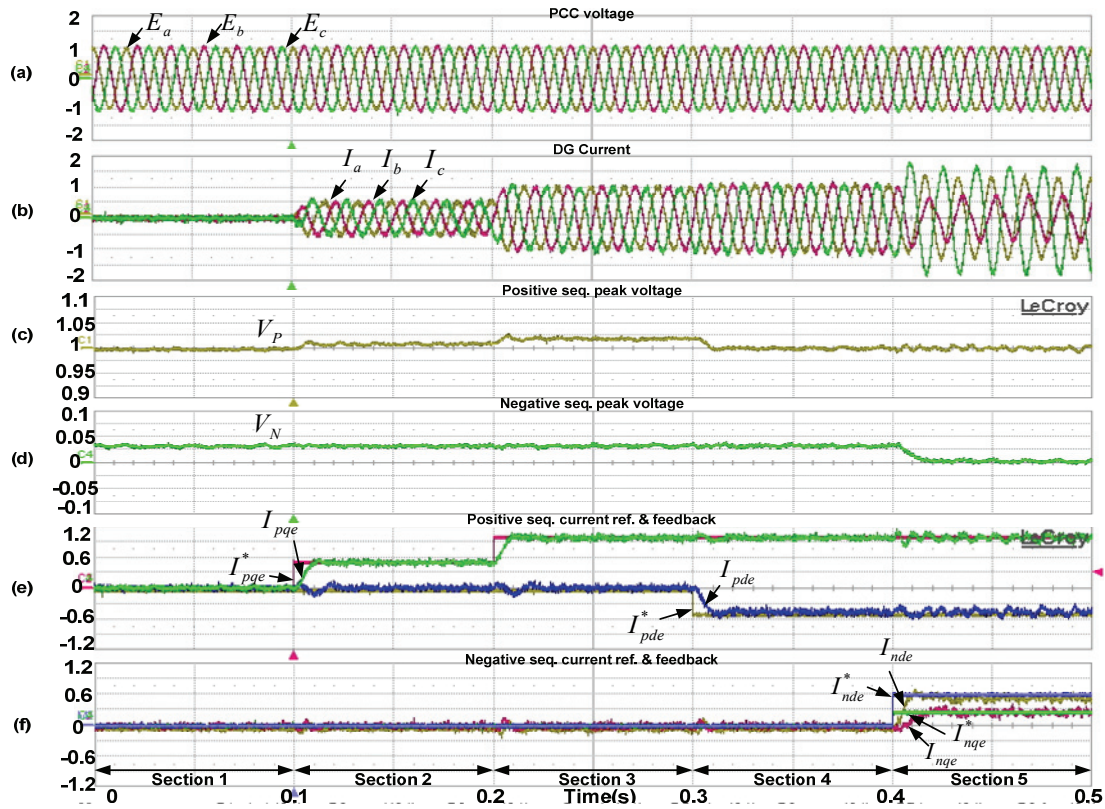
Fig. 8. Experimental results for the injection of currents: (a) PCC voltage of each phase: 0.5pu/div; (b) DG output current of each phase: 0.5pu/div; (c) Positive sequence peak voltage: 0.025pu/div; (d) Negative sequence peak voltage: 0.025pu/div; (e) Positive sequence current reference and feedback: 0.3pu/div; (f) Negative sequence current reference and feedback: 0.3pu/div

scenarios, the positive sequence voltage increases from 1 pu to 1.01 pu and 1.02 pu. In Section 4 of Fig. 8, the calculated current in (7) is injected to the grid in order to compensate the voltage variation. Therefore, the positive sequence voltage is recovered to 1 pu, the conditions without DG q-axis current.

For the unbalance conditions, the unbalance factor of the PCC is 3%, and the phase of the negative sequence voltage vector is 0 degrees. Between Sections 1 to 4 (0 s ~ 0.4 s) of Fig. 8, before the negative sequence current injection, the negative sequence voltage stayed at 0.03 pu. In Section 5, however, the negative sequence current calculated in (8) compensates the negative sequence voltage to 0 pu.

5.3 Current limitation of DG

As shown in Section 5 of Fig. 8, this method requires a high amount of current for compensation. If the DG needs all current components, it has to endure about 2 pu peak current. To limit the DG current, the proposed current limitation algorithm is applied, as shown in Fig. 9 and Fig. 10.

Fig. 9 and Fig. 10 show the simulation and experimental results, respectively, of the following: the positive sequence voltage of PCC $\{I_p\}$; the negative sequence

voltage of PCC $\{I_n\}$; the d-q axis positive sequence current commands and responses in the synchronous frame $\{I^*_{pde}, I^*_{pqe}, I_{pde}, I_{pqe}\}$; and the d-q axis negative sequence current commands and responses in the synchronous frame $\{I^*_{nde}, I^*_{nqe}, I_{nde}, I_{nqe}\}$.

In this scenario, for verifying the proposed current limitation strategy, the current limit has increased with a ramp rate 0.35 pu per 0.1 s and an offset 0.35 pu. The DG outputs all currents as shown in Section 5 of Table 2.

In Section 1 of Table 2, there is no current limitation. (The unbalance factor is 3%) In Section 2, the DG is only able to output is the positive sequence active current. When the current limit exceeds 1 pu, the reactive current, I_{pde}, appears as shown in Section 3. In Section 4, a positive sequence current and a negative sequence current are present because the current limit is enough to output the positive sequence current. (The unbalance factor is 0%) Also, this means that a negative sequence current has increased gradually, according to the current limit, at the same rate of d-axis and q-axis. Finally, all currents are outputted with no limitation upon reaching 2 pu of the current limit.

Fig. 10 also shows the current vector diagram of the areas between Section 2 and Section 4. The current vector in Section 2, is aligned to the q-axis of synchronous frame,
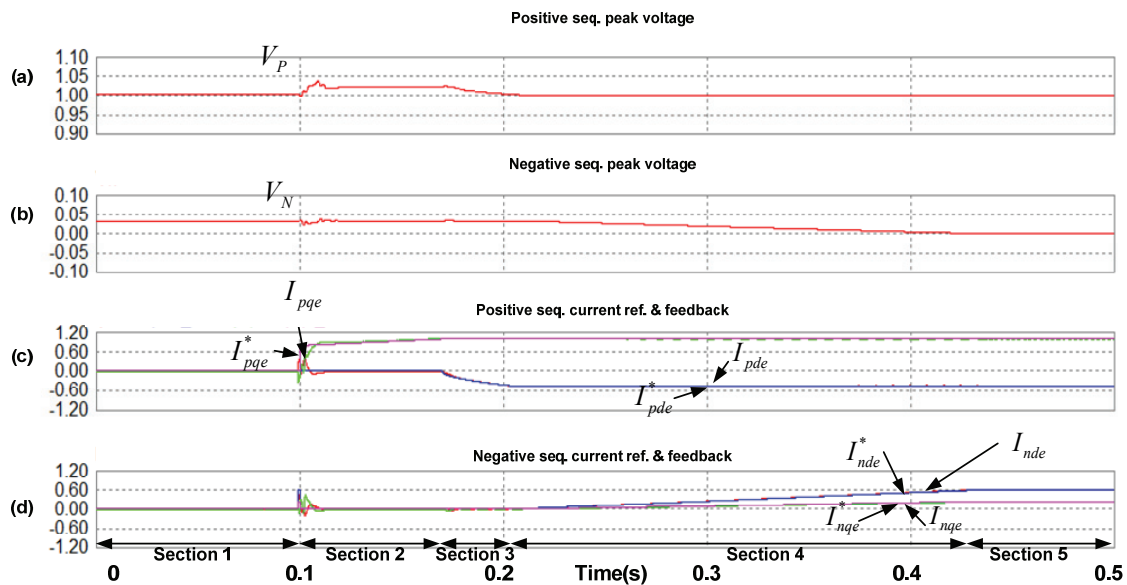
Fig. 9. Simulation results for the injection of currents: (a) Positive sequence peak voltage: 0.05pu/div; (b) Negative sequence peak voltage: 0.05pu/div; (c) Positive sequence current reference and feedback: 0.6pu/div;(d) Negative sequence current reference and feedback: 0.6pu/div
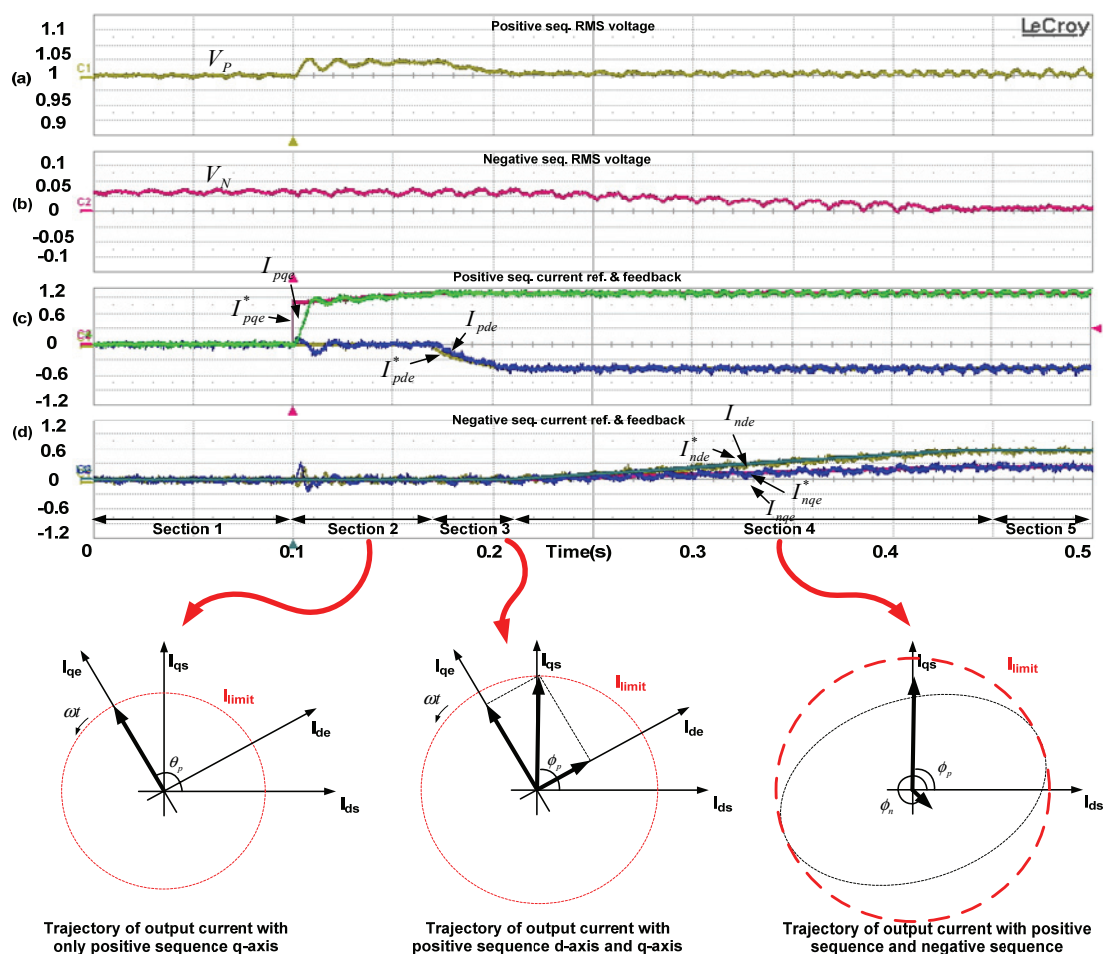
Fig. 10. Experimental results for the injection of currents with the current vector diagram: (a) Positive sequence peak voltage: 0.025pu/div; (b) Negative sequence peak voltage: 0.025pu/div; (c) Positive sequence current reference and feedback: 0.3pu/div; (d) Negative sequence current reference and feedback: 0.3pu/div

because there is only a active current. In Section 3, the current vector has angular degree of freedom with a circle owing to the current vector is composed of active and reactive current. It may also be seen that the current vector in Section 4 has an elliptical trajectory within the current limitation circle. An unbalance factor is reaching for 0% from 3% in this section.

6. Conclusion

This paper proposes a compensation method for the voltage variation at the PCC caused by the active power fluctuation of the grid-connected inverter for DG. This method can also support the PCC voltage under unbalanced voltage conditions at the PCC. It was determined in this paper that the amount of the voltage deviation depends on the positive sequence output current of the DG, the equivalent line impedance, and the load impedance.

Since this proposed algorithm attempts to solve voltage variation issues by using only the DG itself, the use of a PI voltage controller is not required. Based on the results of this study, it was also determined that the proposed algorithm can be used to improve the power quality of DG integration.

Additionally, this paper suggests a current limitation strategy that considers the limitations of the DG capacity. Because of the high output currents that may result from the compensation method used in this paper, the suggested current limitation strategy bases its decision on a predetermined prioritization of the following output currents: active current (the positive sequence q-axis current), the reactive current (the positive sequence d-axis current), and the d-axis and q-axis negative sequence currents. If, for example, the voltage at the PCC undergoes low voltage conditions, the strategy will change the priority of the output currents. The performance of this strategy was demonstrated and verified using computer simulations and experiments.

Acknowledgements

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