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# CMOS 120 GHz Phase-Locked Loops Based on Two Different VCO Topologies

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## Abstract

This work describes the development and comparison of two phase-locked loops (PLLs) based on a 65-nm CMOS technology. The PLLs incorporate two different topologies for the output voltage-controlled oscillator (VCO): LC cross-coupled and differential Colpitts. The measured locking ranges of the LC cross-coupled VCO-based phase-locked loop (PLL1) and the Colpitts VCO-based phase-locked loop (PLL2) are 119.84–122.61 GHz and 126.53–129.29 GHz, respectively. The output powers of PLL1 and PLL2 are −8.6 dBm and −10.5 dBm with DC power consumptions of 127.3 mW and 142.8 mW, respectively. The measured phase noise of PLL1 is −59.2 at 10 kHz offset and −104.5 at 10 MHz offset, and the phase noise of PLL2 is −60.9 dBc/Hz at 10 kHz offset and −104.4 dBc/Hz at 10 MHz offset. The chip sizes are 1,080 μm × 760 μm (PLL1) and 1,100 μm × 800 μm (PLL2), including the probing pads.

**Key Words**: CMOS, Frequency Doubler, Phase-Locked Loop (PLL), Signal Source, Voltage-Controlled Oscillator (VCO).

## I. INTRODUCTION

The increasing demand for high data rates in wireless communication systems has led to the extension of the carrier frequency up to the millimeter- and submillimeter-wave bands [1, 2]. At the same time, to implement a quadrature-phase-based communication system, such as a QPSK or QAM, a local oscillator with a low phase noise is essential. Consequently, the need for a precise oscillation frequency control with a low in-band phase noise at an increased frequency has been growing, and this oscillation frequency control calls for a phase-locked loop topology (PLL) operating at the millimeter- and submillimeter-wave bands. The semiconductor technologies for this purpose have multiple options, but the Si CMOS technology is preferred in many cases because it offers a fully integrated solution with low cost, low DC power consumption, and high integration level. For this reason, recent attempts, including those by the authors [3, 4], have been made to develop CMOS PLLs operating above 100 GHz. In the current work, Si CMOS PLLs operating near 120 GHz are successfully developed, and they exhibit improvement in both output power and locking range compared with the previous result [5]. The Si CMOS PLLs were achieved through a different approach taken for the voltage-controlled oscillator (VCO), a key component of high-frequency PLLs. Two types of VCOs are constructed in this work, an LC cross-coupled VCO and a differential Colpitts-based VCO. Subsequently, two PLLs based on the two VCOs, designated as PLL1 and PLL2, respectively, are developed and their performances are compared.

## II. CIRCUIT DESIGN

A PLL is a feedback system in which the frequency of a VCO output signal is divided by a divider chain, and its signal

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phase is controlled by comparing it with a reference signal. Fig. 1 shows the block diagram of the proposed 120 GHz PLLs. It consists of a VCO, an injection-locked frequency divider (IL-FD), a 9-stage current-mode logic (CML) divider chain, a falling-edge phase frequency detector (FE-PFD), a charge pump (CP), and a second-order loop filter. The main difference between the two PLLs is the VCO structure employed inside each PLL. The description of each circuit component is as follows.

The VCO is a main component of a PLL, and it plays a critical role in high-frequency applications. The output power of the VCO determines the PLL output power level, and the locking range of the PLL is dictated by the VCO tuning range. For the PLL to be favorably used in high data rate wireless communication, the phase noise performance is critical and is affected by that of the VCO. Although the in-band phase noise of the PLL is effectively suppressed in the feedback loop, the out-band phase is still determined by the VCO phase noise.

Two VCOs are developed in this work, one with an LC cross-coupled VCO (VCO1) and the other with a differential Colpitts-based VCO (VCO2). For both VCOs, a frequency doubler is internally integrated to obtain a 2nd harmonic signal above 100 GHz for the PLL output. Compared with the case based on the fundamental-mode VCO, this harmonic approach can take advantage of a small phase noise at a low-frequency VCO operation, and it benefits the 2nd harmonic output signal of the frequency doubler. Moreover, the harmonic approach enables the fundamental signal to be taken for the frequency divider input, which saves one stage of the frequency divider chain. The schematics of the VCOs are shown in Fig. 2. The dual-mode VCOs provide the primary and secondary outputs, which correspond to the 2nd harmonic signal ($2f_0$) near 120 GHz and the fundamental signal ($f_0$) around 60 GHz, respectively.

Fig. 2(a) illustrates the schematic of VCO1. A pair of varactors with a size of 0.25 μm × 6 μm is integrated with the VCO core to control the oscillation frequency, and source-follower buffers (M3, M4) are connected for the fundamental output signal ($f_0$). The fundamental signal, which is a differential signal of the VCO core, is injected into the input of the frequency

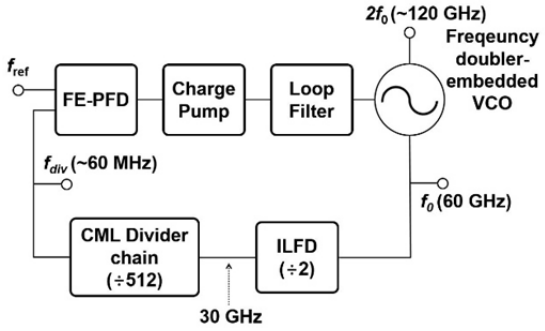



Fig. 1. Block diagram of the PLLs developed in this work.

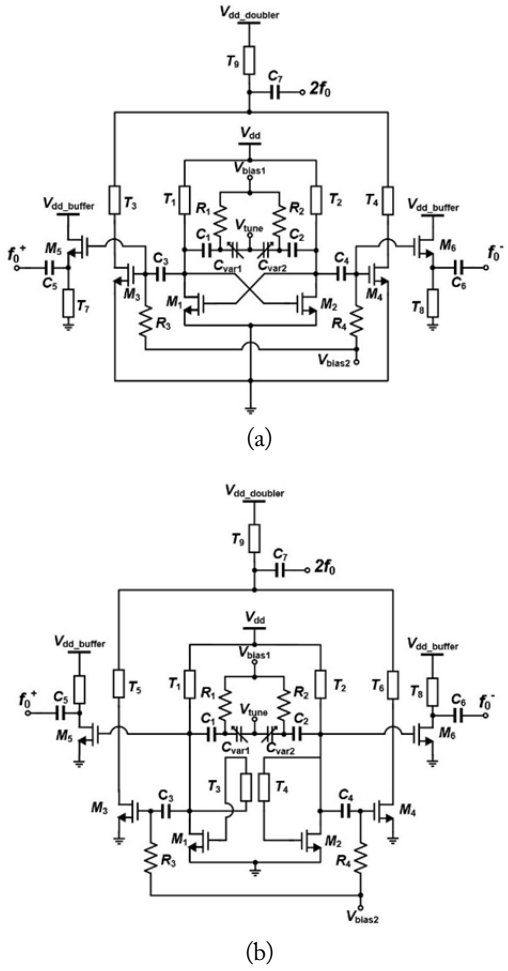
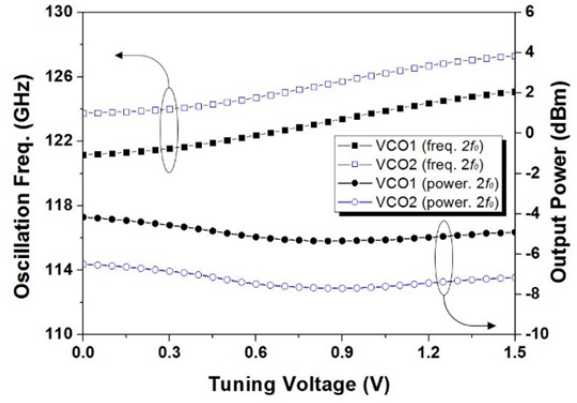


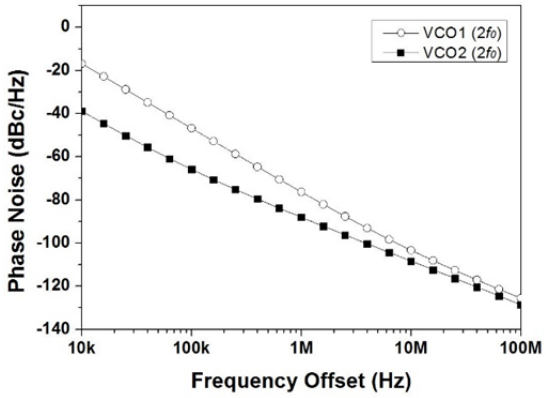

Fig. 2. Circuit schematics of the VCOs. (a) LC cross-coupled VCO and (b) differential Colpitts VCO.

doubler based on the common-source configuration. The 2nd harmonic signal ($2f_0$) is extracted from the common drain node of the frequency doubler, at which the fundamental signal is canceled out. Fig. 2(b) shows the schematic of VCO2. Colpitts-based oscillators are known to benefit from the excellent phase noise performance and are thus suitable for generating high frequency signals [6]. As the fundamental signal should be differential because it leads to the differential frequency doubler, the Colpitts-based VCO is made differential by adopting a gate–drain feedback topology. The fundamental signal currents are coupled in the gate–drain transmission line ($T_3$, $T_4$), and they are configured in the opposite direction for the two output signals to obtain differential phases. A pair of common-source buffers is employed to enhance the fundamental output power. The integrated frequency doubler is similar to the one used for the VCO1.

The simulated oscillation frequency, output power, and phase noise of the VCOs are plotted in Fig. 3. As shown in Fig. 3(a), the simulated oscillation frequency ($2f_0$) of VCO1 varies from 121.2 GHz to 125.1 GHz and that of VCO2 varies from 123.7 GHz to 127.3 GHz, with the tuning voltage swept from 0 V to




(a)




(b)

Fig. 3. Comparison of the LC cross-coupled VCO (VCO1) and the differential Colpitts VCO (VCO2) based on simulation. (a) Oscillation frequency and output power. (b) Phase noise.

1.5 V. The output power of VCO1 is −4 dBm to −6 dBm, which is slight higher than the −6.7 dBm to −7 dBm observed for VCO2. The comparison of the simulated phase noise at $2f_0$, as shown in Fig. 3(b), indicates that VCO2 exhibits a lower phase noise than VCO1 by up to about 20 dB. The difference is more significant for lower frequencies. Although the 2nd harmonic signal ($2f_0$) is the output of the PLL, the fundamental signal ($f_0$) is the one that drives the input of the frequency divider. Simulation results show that the output power of the fundamental signal around 60 GHz is about 0 dBm for both VCOs; this value is high enough to drive the first stage of the frequency divider chain.

Among various topology options for frequency dividers, ILFDs have recently emerged as a viable option for millimeter-wave applications because of their high operation frequency with reasonable power consumption. As the frequency of the signal injected into the divider chain in the PLL in this work is high at around 60 GHz, an ILFD is adopted for the first stage of the frequency divider chain. Fig. 4 is the circuit schematic of the V-band ILFD used in this study. The frequency alignment with the VCO is a key issue because of the narrow locking

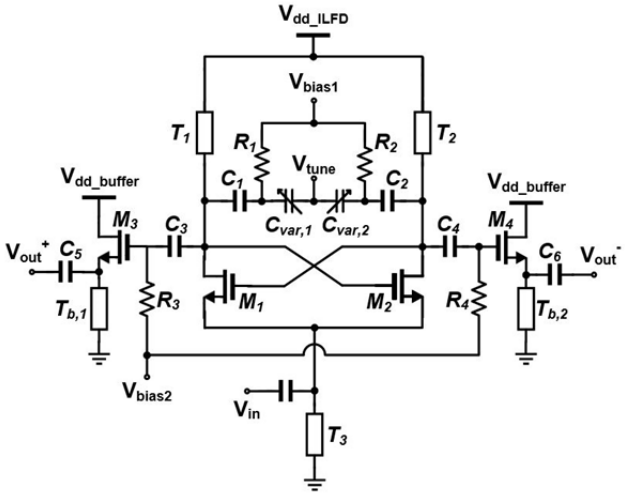


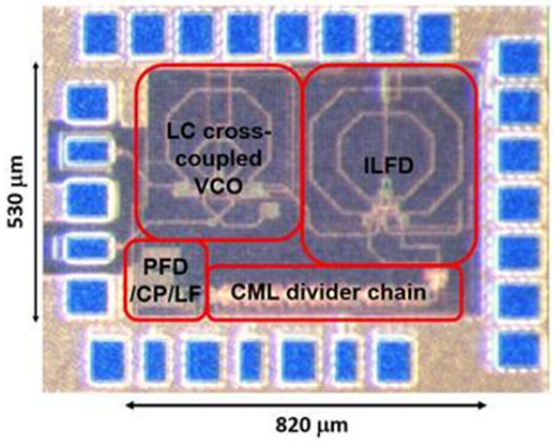

Fig. 4. Circuit schematic of the ILFD.

range of the ILFD at high frequency. Therefore, an LC cross-coupled oscillator-based ILFD, which has a similar structure as the VCO and is suitable for frequency alignment, is adopted. A pair of varactors is integrated with the circuit core to enable the tuning of the locking frequency. The oscillator core embedded in the divider oscillates near the half (near 30 GHz) of the input signal, which is injected into the common source node of $M_1$ and $M_2$. The current of the oscillator core is reduced to the minimum value required for ILFD oscillation, which is expected to enhance the locking range of the ILFD [7].

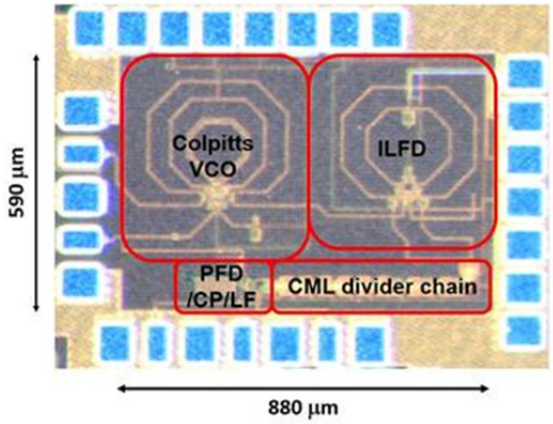
The remaining part of the frequency divider chain is implemented with a 9-stage divide-by-two CML divider, which has a division ratio of 512. Thus, the total division ratio of the divider chain is 1024, decreasing the fundamental frequency $f_0$ to around 60 MHz. The input signals injected into the first three CML stages are relatively high (30, 15, and 7.5 GHz) for the CML operation; therefore, special care is taken to optimize the transistor size and bias for high-speed operation. As for FE-PFD, CP, and LF, which constitute the remaining part of the PLL, topologies similar to those in previous work are used [5]. Note that the circuit blocks other than the VCO are shared between the two PLLs.

## III. Experimental Results

The two PLLs were fabricated using the Samsung 65-nm 1P8M CMOS technology, which exhibits $f_T/f_{max}$ of 200/220 GHz. Fig. 5 shows the chip photos of the completed PLLs. The total chip sizes of PLL1 and PLL2 were 1,080 μm × 760 μm and 1,100 μm × 800 μm, respectively, including the probing pads. The core sizes, excluding the probing pads, were 820 μm × 530 μm (PLL1) and 880 μm × 590 μm (PLL2). The individual test circuits of the VCOs and the ILFD were fabricated to characterize their performances.



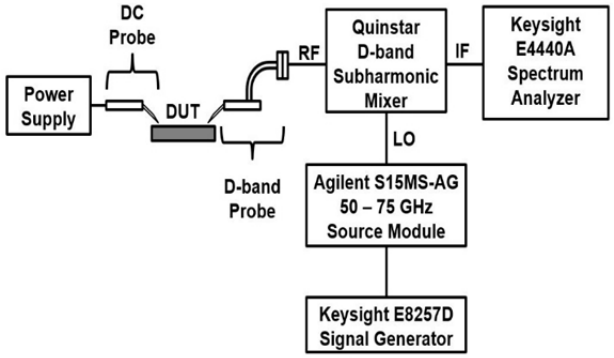

(a)



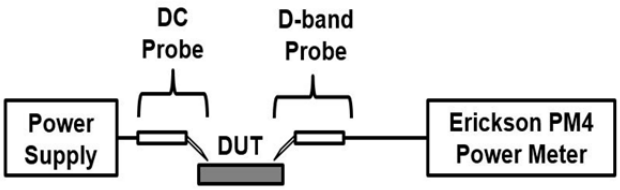

(b)

Fig. 5. Chip photograph of the fabricated PLLs. (a) PLL1 (with LC cross-coupled VCO). (b) PLL2 (with Colpitts VCO).

First, the individual VCOs were characterized, and the results were described. Fig. 6 shows the setups for measuring the frequency spectrum and the output power of the two VCOs. The output spectrum of each VCO was measured by an Agilent E4407B spectrum analyzer after a frequency down-conversion with a QuinStar D-band subharmonic mixer, in which an on-chip probing was employed with a GGB D-band (110–170 GHz) waveguide probe (Fig. 6(a)). An Agilent 50-75 GHz signal source module, which multiplies the signal from a Keysight E8257D signal generator, served as the local oscillator for the down-conversion. The output power was measured through an Erikson PM4 power meter without a frequency down-conversion (Fig. 6(b)). The measured tuning range and the output power variation of the VCOs are shown in Fig. 7. With $V_{\_tune}$ swept from 0 V to 1.5 V, the oscillation frequency ($2f_0$) of VCO1 and VCO2 increased from 118.1 GHz to 121.2 GHz and from126.2 GHz to 129.1 GHz, respectively. The output powers were measured at about –8 dBm for VCO1 and –10.5 dBm for VCO2, with a calibrated power loss of the D-band probe (approximately 2.5 dB). The output powers of the




(a)




(b)

Fig. 6. Measurement setups for the VCOs: (a) spectrum measurement and (b) power measurement. The same setup is used for PLL measurement, except for a separate reference signal applied to the DUT from a signal generator.

fundamental signal ($f_0$) of the VCOs were measured at around 0 dBm for both cases across the entire tuning range. The DC power consumptions of the two VCOs were 66 mW and 76.5 mW, respectively, and they include the consumption in the VCO core, frequency doubler, and fundamental buffers.

Second, the ILFD was characterized for the input sensitivity and the locking range. The input signal ($f_0$ = approximately 60 GHz) provided by an Agilent 50–75 GHz source module was injected into the ILFD, and the divided output signal was measured with an Agilent E4407B spectrum analyzer. The measured sensitivity curves for the ILFD with a tuning voltage

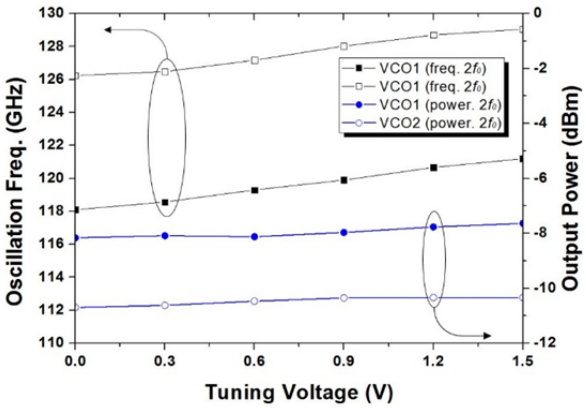



Fig. 7. Measured tuning range and the output power of the fabricated VCO.

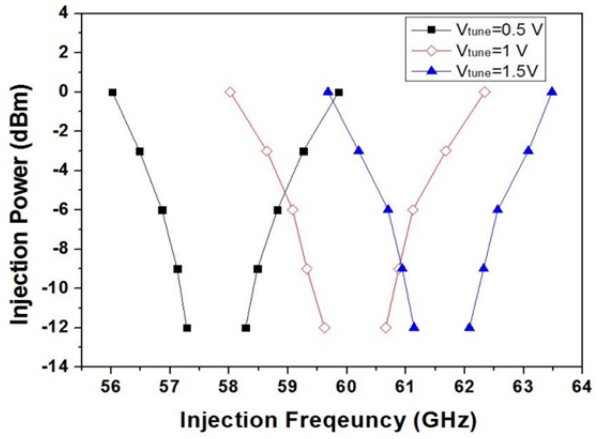
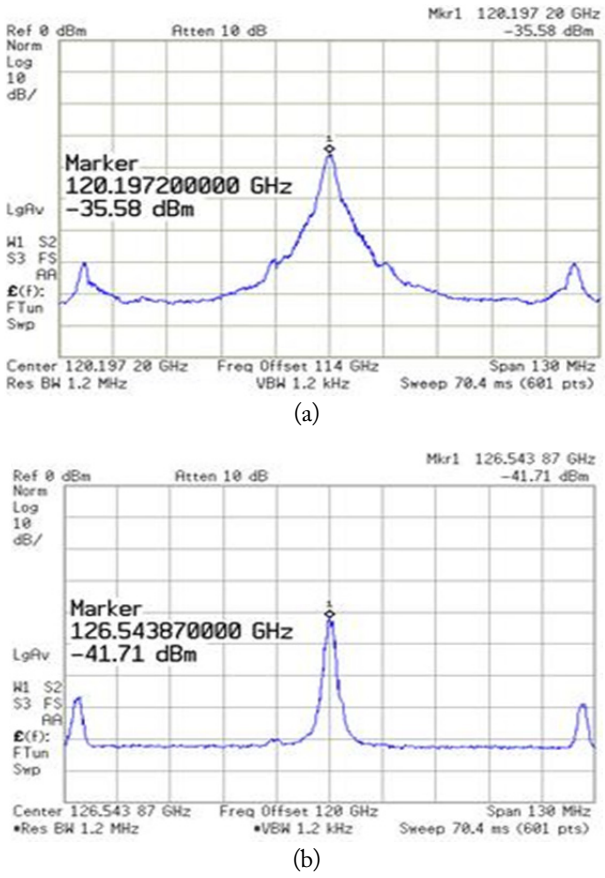



Fig. 8. Measured input sensitivity curves of the V-band ILFD with bias variation.



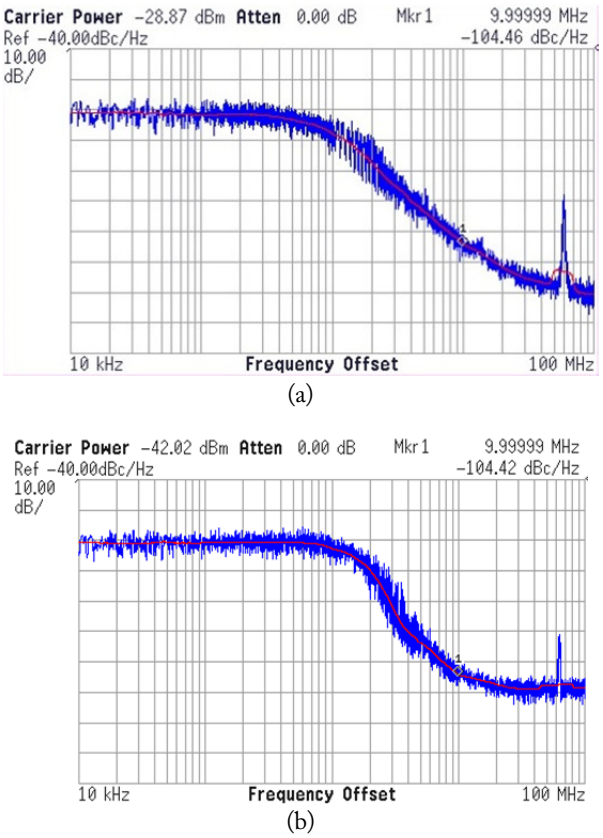

(a)

(b)

Fig. 9. Measured output spectra of the fabricated PLLs: (a) PLL1 and (b) PLL2. The resolution bandwidth is 1.2 MHz, and the span is 130 MHz.

variation are shown in Fig. 8. Given that the measured input signal from the VCO injected into the 60 GHz ILFD was around 0 dBm, the locking range was estimated to be around 10 GHz, a reasonably broad value to achieve a locking. The ILFD core and the buffer both drew 6 mA from a 0.8 V and a 1 V supply voltage, respectively.

Finally, the integrated PLLs were characterized. The PLL measurement setup was similar to that of the VCOs, in which the 2nd harmonic output signal was down-converted and measured by the same spectrum analyzer. One difference from the VCO test setup is the injection of the reference signal near 60 MHz into the FE-PFD; this signal is generated by an Agilent E8247C signal generator. Fig. 9 shows the measured output spectra of the fabricated PLLs. The measured locking range of PLL1 was 119.84–122.61 GHz and that of PLL2 was 126.53–129.27 GHz, and they were included in the entire tuning range of the associated VCOs. In the spectrum, reference spurs at around 60 MHz were observed on both sides of the center frequency; this outcome could be considered evidence of the locked state. Fig. 10 shows the measured phase noise plot of the PLLs in the locked state. The phase noise of PLL1 was measured as −59.2 at 10 kHz offset and −104.5 at 10 MHz offset. For PLL2, −60.9 dBc/Hz and −104.4 dBc/Hz were obtained for 10 kHz and 10 MHz offsets, respectively. Deducing that the phase noise performance shows little difference is reasonable. Both plots show reference spurs at the same frequency offset as that observed in the output spectrum in Fig. 9. The measured output powers were −8.6 dBm and −10.5 dBm for PLL1 and PLL2, respectively, at around the operation frequency. The total DC power consumptions were 127.3 mW for PLL1 and 142.8 mW for PLL2. In terms of the output power and the DC-to-RF efficiency, PLL1 performed slightly better than




(a)

(b)

Fig. 10. Measured phase noise of the fabricated PLLs: (a) PLL1 and (b) PLL2.

Table 1. Comparison of the CMOS PLLs operating over 100 GHz

| | [3] | [4] | [5] | This work | |
|---|---|---|---|---|---|
| Technology | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS | 65-nm CMOS |
| VCO type | LC cross-coupled | VCO with mixer | LC cross-coupled | LC cross-coupled | Colpitts |
| Division ratio | /256 | /8 | /1,024 | /1,024 | /1,024 |
| Reference (MHz) | 406 | 130 | 59.06 | 59.18 | 62.57 |
| Locking range (GHz) | 103–104.6 (1.5 GHz) | 162–164 (2 GHz) | 121.9–122.2 (0.3 GHz) | 119.8–122.6 (2.8 GHz) | 126.5–129.8 (2.8 GHz) |
| Phase noise (dBc/Hz) | −85.37 (@ 1 MHz) | −80.41 (@ 1 MHz) | −102.5 (@ 10 MHz) | −104.5 (@ 10 MHz) | −104.4 (@ 10 MHz) |
| RF output power (dBm) | −23.1 | −19.5 | −8.6 | −8.6 | −10.5 |
| DC power consumption (mW) | 63 | 24 | 82.9 | 127.3 | 142.8 |
| Area ($mm^2$) | 0.84 | 0.96 | 0.76 | 0.82 | 0.88 |

PLL2. Table 1 summarizes the performance of the PLLs based on the 65-nm CMOS technology operating above 100 GHz.

## IV. Conclusion

Two PLLs based on the 65-nm CMOS technology operating near 120 GHz are developed. Each PLL adopts a different VCO topology, either the LC cross-coupled or the Colpitts, and the measured performances are compared. This work not only demonstrates the feasibility of implementing the PLLs over 100 GHz based on the CMOS technology but also compares the two popular topologies for the VCOs incorporated into the PLLs. The developed PLLs can be adopted as a stable signal source for various applications beyond 100 GHz, including D-band communication systems.

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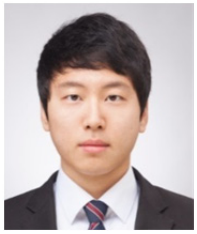

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