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Comparison of Two Layout Options for 110-GHz CMOS LC Cross-Coupled Oscillators

Doyoon Kim · Jae-Sung Rieh*

Abstract

Two 110-GHz oscillators have been developed in 65-nm CMOS technology. To study the effect of layout on the circuit performance, both oscillators had the same LC cross-coupled topology but different layout schemes of the circuit. The oscillator with the conventional cross-coupled design (OSC1), showed an output power of –3.9 dBm at 111 GHz with a phase noise of –75 dBc/Hz at 1-MHz offset. On the other hand, OSC2, with a modified cross-coupled line layout, generated an output power of –2.0 dBm at 117 GHz with a phase noise of –77 dBc/Hz at 1-MHz offset. The result indicates that the optimized layout can improve key oscillator performances such as oscillation frequency and output power.

Key Words: Layout, LC Cross-Coupled, Oscillators, Signal Generation, 65-nm CMOS.

I. INTRODUCTION

With the recent advancements in device technology, systems operating at a frequency exceeding 100 GHz are being widely studied for various high-frequency applications, including imaging and communication [1, 2]. One of the difficulties in designing such a system is the presence of unwanted parasitic components that critically affect the system performance [3]. Therefore, given such an effect, we can expect the performance of designed circuits to be significantly affected by the layout of the circuits. In this study, we investigated the actual effect of layout on the circuit performance of two 110-GHz oscillators fabricated in Samsung 65-nm CMOS technology.

II. CIRCUIT DESIGN

To study the effect of layout on circuit performance, we designed and implemented two LC cross-coupled oscillators (OCS1 and OCS2) with different layout schemes. Fig. 1 shows the schematic of the oscillator design, which is identical for the two oscillators on the circuit level. The LC cross-coupled oscillator is composed of four transistors, two (M_1 and M_2) for the oscillator core and the other two (M_3 and M_4) for the buffer.

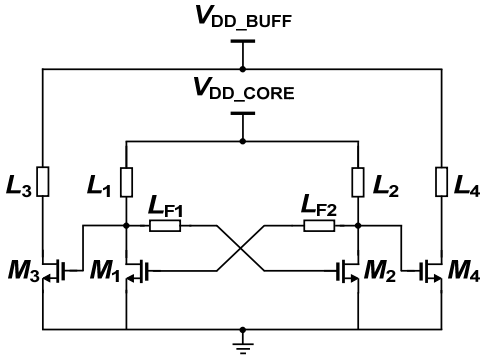

Fig. 1. Schematic of the oscillators.

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School of Electrical Engineering, Korea University, Seoul, Korea.
*Corresponding Author: Jae-Sung Rieh (e-mail: jsrieh@korea.ac.kr)

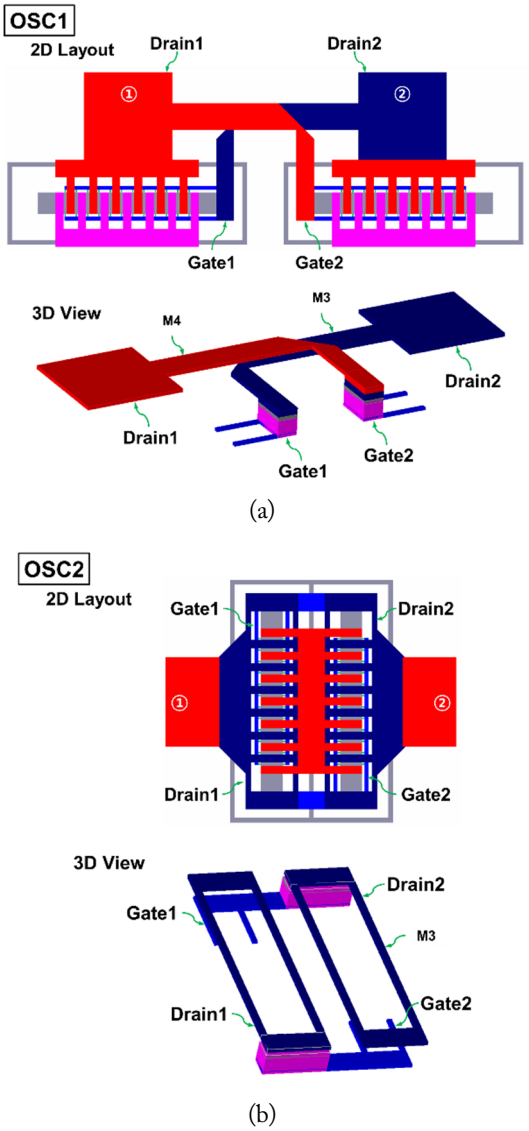

Fig. 2. Core drawings of OSC1 (a) and OSC2 (b).

Based on the schematic design, we drew two different core layouts, which are expected to critically affect the oscillators' electrical performances. The layout details of the two core drawings are depicted in Fig. 2. For the core of OSC1, as shown in Fig. 2(a), the cross-coupled lines are placed outside the device area, which is the conventional approach. For the implementation, since a line crossing is inevitable, two metal layers of M3 and M4 are used to interconnect the gate and the drain of the other device. For the core of OSC2, as shown in Fig. 2(b), the cross-coupled lines are formed inside the device area. This case takes advantage of the symmetry in the layout of the offered transistors in a process design kit (PDK) and uses a single metal layer M3 for the cross-coupling. Such a modification is expected to improve the circuit performance.

First, as in [4], for an LC cross-coupled oscillator, w_{OSC} can be obtained as follows:

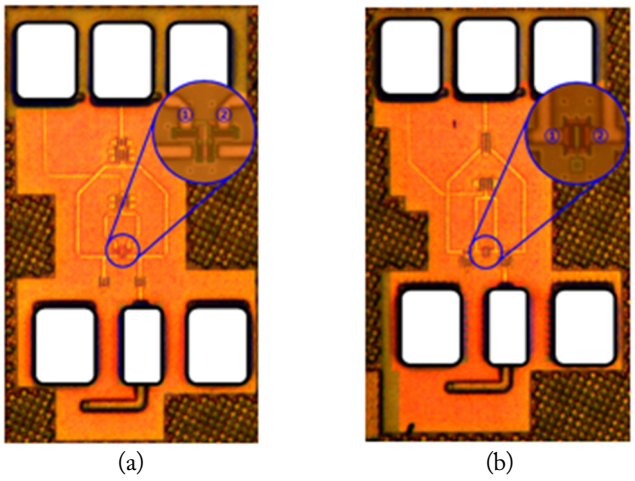

Fig. 3. Chip photos of (a) OSC1 and (b) OSC2. The core regions are zoomed to better show the orientation of the core device.

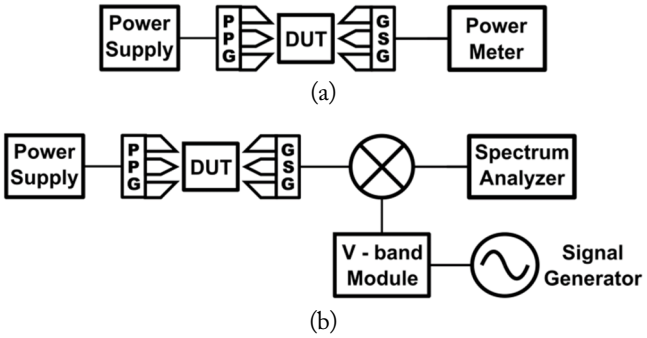

Fig. 4. Measurement setups: (a) power and (b) spectrum/phase noise.

$$w_{OSC} = \sqrt{\frac{1}{(L_F + L_D)}\left(\frac{1}{C_F} + \frac{1}{C_p}\right)}\,. \tag{1}$$

From (1), we can see that by reducing L_F, higher oscillation frequency, w_{OSC}, can be obtained for OSC2. Second, since the cross-coupled metal length is reduced, parasitic resistance, R_p, will also reduce, which will lead to enhancement of the resonator's Q-factor. The enhancement in Q-factor, in turn, will increase the output power. Lastly, as shown in Fig. 2(b), perfect symmetry can be obtained as a single metal layer is used for cross-coupling, providing advantages of a fully differential pair for OSC2.

III. Measurement Results

The two 110-GHz oscillators were fabricated with Samsung 65-nm CMOS process, which has f_T/f_{max}=200/220 GHz. The chip photos for the fabricated oscillators are shown in Fig. 3. Each oscillator occupies an area of 540 μm × 320 μm, including probing pads for DC supply and RF measurements.

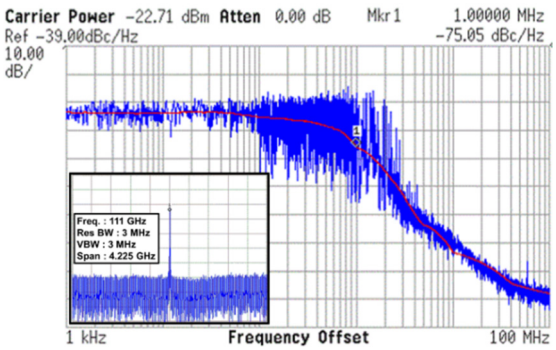

Fig. 5. OSC1 measurement results.

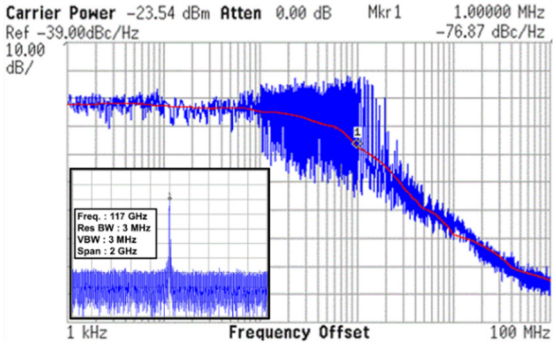

Fig. 6. OSC2 measurement results.

The electrical performances were characterized by measuring the output power, spectrum, and phase noise. The measurement setups are described in Fig. 4. For the power measurement, a VDI PM5 power meter was directly connected to the DUT via a GGB D-band GSG probe. For the spectrum and phase noise measurement, a VDI WR6.5 subharmonic mixer, an Agilent V-band source module, an Agilent E8247C signal generator, and an Agilent E4440A spectrum analyzer were used.

OSC1 generated an output power of −3.9 dBm at 111 GHz and showed a phase noise of −75 dBc/Hz at 1-MHz offset. The results are shown in Fig. 5. OSC2 generated an output power of −2 dBm at 117 GHz and a phase noise of −77 dBc/Hz at 1-MHz offset. The results are shown in Fig. 6. The output power values were calibrated with a probe loss of 2.5 dB (from data sheet). Table 1 shows the summarized oscillator performances. The results clearly indicate that the modified layout with improved symmetry and reduced coupling metal line length leads to enhancement in both output power and phase noise.

Table 1. Measured performance summary of the oscillators

Circuit	Output power (dBm)	Frequency (GHz)	Phase noise (dBc/Hz)
OSC1	−3.9 (−2.4)	111 (117)	−75 @ 1-MHz
OSC2	−2.0 (−1.5)	117 (128)	−77 @ 1-MHz

Numbers in parenthesis for comparison are simulated values.

IV. Conclusion

Two LC cross-coupled oscillators fabricated in Samsung 65-nm CMOS technology were developed and compared. The oscillator with a modified layout (OSC2) showed enhanced performance compared with the conventional layout (OSC1). The improvement is ascribed to improved symmetry as well as reduced inductance and parasitic line resistance.

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