Compensation Technique for Current Sensorless Digital Control of Bridgeless PFC Converter under Critical Conduction Mode

Tae-Hun Kim* and Woo-Cheol Lee†

Abstract – Critical conduction mode (CRM) operation is more efficient than continuous conduction mode (CCM) operation at low power levels because of the valley switching of switches and elimination of the reverse recovery losses of boost diodes. When using a sensorless digital control method, an error occurs between the actual and the estimated current. Because of the error, it operates as CCM or discontinuous conduction mode (DCM) during CRM operation and also has an adverse effect on THD of input current. In this paper, a current sensorless technique is presented in an inverter system using a bridgeless boosted power factor correction converter, and a compensation method is proposed to reduce CRM calculation error. The validity of the proposed method is verified by simulation and experiment.

Keywords: Bridgeless boost converter, Current sensorless, Error compensation, Digital control

1. Introduction

Traditional boost power factor correction (PFC) converters have the disadvantage of low efficiency because they use a bridge rectifier. To overcome this drawback and to develop a high-efficiency PFC converter, many studies have been conducted on the bridgeless PFC converter family [1-4]. Basic bridgeless PFC boost converters are simple, have the fewest number of devices, are cost effective, and have high efficiency, but common-mode (CM) noise resulting from CM voltage causes CM electromagnetic interference (EMI) [1-3]. Among the various bridgeless PFC converter families, the two-boost-circuit PFC is mainly used because it can solve the EMI problem and has simple circuit structures using two boost circuits [4].

Critical conduction mode (CRM) operation and discontinuous conduction mode (DCM) operation offer higher efficiency than continuous conduction mode (CCM) operation at low power levels because of the valley switching of the switch and elimination of the reverse recovery losses of the diodes [4-8]. However, they are mainly used at low power because the current peak value is increased compared to CCM. CRM is used at high power level than DCM because the current peak is smaller than DCM and current THD of CRM is also superior [6, 7]. Fig. 1 shows a basic bridge-boost PFC converter operating in CRM. To implement CRM operation, zero or peak current sensing is required, and CRM has the disadvantage that the switching frequency varies depending on the input voltage and power [7, 8].

With the development of digital devices, many systems have been digitized and much research on the digitization of PFC converters has been conducted [9-11]. In [11], a study on the digital control of the CRM method was carried out. The output characteristics of the CRM method depend on the current sensing method and the PWM method. To implement CRM, a fast AD-converter is required and the cost increase because CRM operates at a variable frequency [12]. The digital control system has an advantage that sensorless control can be introduced. The current sensorless control has a significant cost advantage as eliminating the current sensor and the ad converter [13]. Errors occur between real and estimated current when implemented using a sensorless digital controller or digital pulse width modulation (DPWM). Due to this error, the switch can not be turned on at zero current which may result in CCM or DCM. Therefore, the error negatively affects the input current THD and compensation is required.
Digital controller should be designed by considering circuit characteristics such as PWM delay and effect of the parasitic components [14-15]. Techniques such as parameter tuning are used to eliminate errors of digital implementation, but these compensation methods require a current sensor [15]. A study to compensate for the effect of voltage drop due to parasitic component in CCM sensorless control was performed in [16]. In [17], a sensorless control using observer for CCM and DCM was implemented. In previous studies, current sensorless control using current observer, and error compensation method by voltage drop by equivalent series resistor of the inductor, diode conduction voltage, and on-state MOSFET resistor have been proposed. One of the causes of the error in CRM calculations is the resonance caused by the parasitic capacitance of the semiconductor and inductance of the boost inductor. The resonance occurs at peak current and valley current during switching. Previous studies have analyzed the valley switching in detail [6]. Resonance at peak current delays the discharge time of the current and cause CCM operation. Around the zero-crossing of the voltage, the magnitude of the current is small and the frequency becomes high. At this time, the error caused by the resonance becomes large after the peak current switching. Therefore, the current waveform can be improved by compensating the error caused by the resonance at the peak current. In this paper, a study was conducted to implement sensorless control under CRM. Sensorless method and error compensation method that can be used in PFC with inverter system are proposed. Much researches have been done in CCM and DCM, and sensorless control and error compensation techniques for CRM should be studied. In this paper, a sensorless method for CRM is proposed. For the CRM implementation, zero current detection is required. Current sensorless requires estimation method because it does not receive zero current information. The estimated current may be inaccurate due to errors caused by the parasitic components. Therefore, a compensation method is indispensable for sensorless control. In this paper, a compensation method for compensate the error caused by the resonance of parasitic components. The input current peak value is estimated and used for current control and error compensation. The validity of the proposed method is verified by simulations and experiments on a prototype 250-W class PFC inverter system.

2. Two-boost PFC Converter

Fig. 2 shows a two-boost-circuit PFC converter. The two-boost-circuit PFC converter has the same switching pattern as the basic bridgeless boost PFC converter. Two additional diodes and one inductor are required in addition to the circuit, but the EMI problem can be solved and the two inductors have better thermal performance compared to that of a single inductor [2].

The dotted line in Fig. 2 represents the parasitic capacitance. The parasitic capacitance of the semiconductor device can cause resonance with the inductor of the boost converter. For CRM operation, the switches should be turned on at zero current and turned off at peak current. Therefore, resonance occurs at zero current and peak current. If the current in the inductor is reduced to zero, it can be valley-switched by resonance when the switch is turned on [4]. At this time, all LC components cause resonance. When the PFC current reaches to peak, the switch is turned off and the current is decreases linearly. The slope of current according to switching state is as:

\[ \Delta L_{on} = \frac{V_{in}}{L_{boost}} \Delta t \]  \hspace{1cm} (1)
\[ \Delta L_{off} = \frac{V_{in} - V_{dc}}{L_{boost}} \Delta t \]  \hspace{1cm} (2)

The on, off time in the CRM operation can be calculated using the following equations and the DPWM can be implemented [12]:

\[ T_{on} = \frac{2P_{dc}L_{boost}}{\eta V_{rms}^2} \]  \hspace{1cm} (3)
\[ T_{off} = \frac{L_{boost}I_{pk\_est}(t)}{V_{dc} - V_{in\_pk}\sin(\omega t)} \]  \hspace{1cm} (4)

where

\[ I_{pk\_est}(t) = 2i_{in}(t) = \frac{4P_{dc}}{\eta V_{in}^2}\sin(\omega t) \]  \hspace{1cm} (5)

and

\[ T_s = T_{on} + T_{off} \]  \hspace{1cm} (6)

where \( T_{on} \) is the on time, \( T_{off} \) is the off time, \( T_s \) is the switching period, \( P_{dc} \) is the DC power, \( L_{boost} \) is the inductance of \( L_{boost} \), \( I_{pk\_est} \) and \( V_{in\_pk} \) is the input voltage peak, and \( i_{pk\_est} \) is the inductor current peak.

The boost inductance of the PFC is derived by Eq. 3-6 as:

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In this paper, to use the minimum switching frequency above 15 kHz, the inductance was determined to be 0.9 mH.

3. Peak Current Time Delay Compensation

Errors occur due to the PWM delay, voltage drop or resonance. In this paper, the error caused by the resonance at the peak current is analyzed and a compensation method is presented.

Fig. 3 shows three modes of the PFC converter operation during a positive half period. Based on Fig. 3(a), $Q_1$ is on, and $L_{boost}$ is charged through $Q_1$ and $D_1$. $V_{d1}$ and $V_{q1}$ are the voltages of parasitic capacitance of $D_1$ and $Q_1$, respectively. In this case, $V_{d1}$ has a voltage of $V_{dc}$ and $V_{q1}$ has a voltage of 0. Based on Fig. 3(b), $Q_1$ is off, and $L_{boost}$ discharges through $D_1$ and $D_e$. $V_{d1}$ has a voltage of 0 and $V_{q1}$ has a voltage of $V_{dc}$. Fig. (c) shows a resonance operation mode before switching from the operation modes (a) to (b). When $Q_1$ is turned off, the voltage of $D_1$ is discharged, and the parasitic capacitance of $Q_1$ is charged to $V_{dc}$ and resonance occurs in this process. $L_{boost}$ and the parasitic capacitances of $D_1$ and $Q_1$ cause resonance at the switch turn off instant. Because the resonance current flows through $D_4$, the parasitic component of $D_4$ does not participate in the resonance.

Fig. 4 shows the operation waveform of the PFC converter. When current $i_{boost}$ reaches $i_{Lpk_{est}}$, switch $Q_1$ is off and $i_{L_{boost}}$ should decrease to a constant slope. However, during the time in which $V_{q1}$ is charged and $V_{d1}$ is discharged, the current flowing through the inductor hardly decreases owing to the resonance. Therefore, the time delay $t_d$ occurs, and the off time of $Q_1$ should be longer for the CRM operation. Because the resonance current flows through $D_4$, the parasitic component of $D_4$ does not participate in the resonance. For a negative half period, $L_{boost2}$ and the parasitic capacitances of $D_2$ and $Q_2$ cause resonance at the switch turn off instant. Fig. 4(a) shows the case where the voltage and $i_{Lpk_{est}}$ are high. In this case, turn-off time becomes long. If $i_{Lpk_{est}}$ is large, the slope of $V_{d1}$ and $V_{q1}$ is large and the resonance time is short. However, if $i_{Lpk_{est}}$ is small, the slope of $V_{d1}$ and $V_{q1}$ is small and the resonance time becomes longer, and the delay time $t_d$ affects the current waveform. Fig. 4(b) shows the case where the voltage and $i_{Lpk_{est}}$ are low around zero current. In this case, $V_{q1}$ cannot be charged up to $V_{dc}$, and $Q_1$ turns on again during resonance. $C_{dc}$ can be ignored because it has a very large value compared to the parasitic components. Therefore, the parasitic capacitances of two

\[
L_{boost} = \frac{\eta V_{dc}^2 (V_{dc} - V_{in})}{2 V_{dc} P_{dc} f_s}
\]
semiconductor devices participating in resonance can be considered as being connected in parallel. Thus, the resonance frequency is calculated for \( L_{\text{boost}} \) and \( 2C_p \) as

\[
f_r = \frac{1}{2\pi \sqrt{2C_p L_{\text{boost}}}}
\]

where \( C_p \) is the parasitic capacitance of the semiconductor device.

The LC resonance analysis should be calculated in as simple a manner as possible because the results are complex, and the calculation time for the system can become long. The capacitances of \( D_1 \) and \( Q_1 \) participate in the resonance, and the time during which the voltage of the parasitic capacitance is inverted is much shorter than the resonance period. Therefore, assuming that the current is constant and the voltage of the capacitor is charged from 0 to \( V_{dc} \) during the time delay \( t_d \), it can be approximated by using Eq. (9). Finally, the compensation time \( T_{\text{comp}} \) can be derived as shown in Eq. (12).

\[
i_{\text{Lpk\_est}} = \frac{2C_p dV_c}{dt}
\]

\[
t_d = \int_{0}^{t_d} i_{\text{Lpk\_est}} dt = \frac{2C_p V_{dc}}{t_d}
\]

\[
i_{\text{Lpk\_est}} t_d = 2C_p (V_{dc} - 0)
\]

\[
T_{\text{comp}} = t_d = \frac{2C_p V_{dc}}{i_{\text{Lpk\_est}}(t)}
\]

Therefore, the off time is calculated as

\[
T_{\text{off}} = \frac{L_{\text{boost}} i_{\text{Lpk\_est}}(t)}{V_{dc} - V_{\text{inpk}} \sin(\omega t)} + \frac{2C_p V_{dc}}{i_{\text{Lpk\_est}}(t)}
\]

\[
T_{\text{off}} = \frac{L_{\text{boost}} i_{\text{Lpk\_est}}(t)}{V_{dc} - V_{\text{inpk}} \sin(\omega t)} + \frac{2C_p V_{dc}}{i_{\text{Lpk\_est}}(t)}
\]

4. Proposed Sensorless Control

Fig. 5 shows the structure of the proposed system and Fig. 6 shows the full-bridge inverter circuit. The inverter operates using a conventional sinusoidal PWM. To implement the current sensorless control of the PFC converter, the input current must be estimated. For the estimation of the input current, the DC power of the PFC converter is required.

To control the inverter voltage and current, it is also necessary to detect the inverter current and the output voltage. Using this method, a sensorless control method for estimating the PFC power is proposed. The power and current can be estimated from the output power by the relational expressions

\[
P_{\text{load}} = \eta P_{dc}
\]

\[
V_{\text{out}} I_{\text{id\_est}} = \eta V_{dc} I_{\text{dc\_est}}
\]

\[
I_{\text{id\_est}} = I_{\text{Lpk}} - \alpha C_f V_{\text{inpk}} \cos(\theta)
\]

\[
I_{\text{dc\_est}} = \frac{V_{\text{out}} (I_{\text{Lpk}} - \alpha C_f V_{\text{inpk}} \cos(\theta))}{\eta V_{\text{dc\_ref}}}
\]

where \( I_{\text{id\_est}} \) is the estimated load current, and \( I_{\text{dc\_est}} \) is the estimated DC-link current.

Fig. 7 shows a detailed schematic diagram of the digital controller of Fig. 5. Fig. 7 (a) shows the PFC controller. The controller of the PFC introduced the voltage-current Proportional-Integral (PI) controller. The voltage PI controller outputs the current reference value using the command value and the measured value of the DC-link voltage. The current PI controller controls the PFC output current, where the current estimate \( I_{\text{dc\_est}} \) is used as feedback. Current measurement is required for the CRM control of PFC. To realize the current sensorless control, the output voltage and current used for the inverter control are used to estimate the PFC current. The PI controller controls the DC-link voltage of the PFC and the output of each controller is transferred to the CRM calculation block. In the CRM calculation block, the duty of the PFC is determined from Eq. (3), (13). The phase and magnitude of the input voltage are needed for the phase-locked loop

Fig. 6. Full-bridge inverter circuit

Fig. 7. Schematic of a digital controller: (a) PFC controller; (b) inverter controller
for synchronous detection and for PFC control for synchronous detection. Fig. 7 (b) shows the controller of the inverter. The inverter controller is also composed of a voltage-current PI controller. The measured value of the output voltage and inductor current are used for the feedback of voltage-current PI control and for the $I_{dc_{est}}$. $I_{dc_{est}}$ is obtained by Eqs. (14)-(17). Phase-locked loop (PLL) is used for power factor control and inverter control. The d-q axis transformation uses the all-pass filter as [18]:

$$V_d' = V_{in}$$  \tag{18}

$$V_q' (t) = -kV_q' (t-1) + kV_d' (t) + V_d' (t-1)$$  \tag{19}

where the $k$ is

$$k = \frac{T \omega - 2}{T \omega + 2}$$  \tag{20}

The PLL process is shown in Fig. 8.

5. Simulation

Table 1 shows the parameters of the proposed system. The switching frequency depends on the magnitude of the input voltage and load condition. It changes from 18 kHz to 80 kHz under the full-load condition and changes from 32 kHz to 130 kHz under half load condition. The switching frequency is determined by Eqs. (3), (6) and (13). The resonant frequency is calculated using Eq. (8). The output power is 250 W under the full-load condition.

Fig. 9 shows the simulation waveform of the turn-off time delay resulting from the resonance under the full-load condition. Because of the parasitic component of the semiconductor device, resonance occurs when the switch is turned off. Therefore, the current cannot be discharged immediately and a time delay occurs. Due to the time delay, an error occurs in the off-time between the calculation and the actual current. If the current does not decrease to zero because of the error, the error accumulates and the current rises. When $L_{pk_{est}}$ approaches 0, the delay time increases and the distortion of the current increases. The switching frequency $f_s$ is determined by the inductor, power, and DC-link voltage and operates at 18.94 kHz.

Fig. 10 shows the simulation waveform when the proposed off-time compensation method was used. Fig. 10 (b) shows that the current distortion is reduced by compensating the time delay. The compensation time $T_{comp}$ can be confirmed in Fig. 10(c). In Eq. (6), as the peak current estimation ($I_{pk_{est}}$) approaches to zero, $T_{comp}$ becomes very high, thus $I_{pk_{est}}$ should be limited to 2 $\mu$s, which is one-fourth of the resonance period. At this time, the maximum frequency is reduced to approximately 80 kHz because the off-time became longer, as much as the compensation time.

Fig. 11 shows the waveform at a moment in Fig. 10. $V_d$ represents the voltage of $D_1$, and $V_{q1}$ represents the voltage of $Q_1$. When $Q_1$ is turned off, $I_{boost}$ should decrease to a constant slope. However, because of resonance, $I_{boost}$ is

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<th>Table 1. System parameters</th>
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<tr>
<td><strong>Parameter</strong></td>
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<tr>
<td>Input voltage ($V_{in}$)</td>
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<tr>
<td>DC-link voltage ($V_{dc}$)</td>
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<tr>
<td>Switching frequency ($f_s$)</td>
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<td>Resonance frequency ($f_r$)</td>
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<td>Boost inductor ($L_{boost1,2}$)</td>
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<td>Parasitic capacitance ($C_p$)</td>
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<td>Output power ($P_{load}$)</td>
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almost unchanged until \( V_d \) is discharged to 0 and \( V_q \) is charged to \( V_{dc} \). Because the actual off time is longer than the calculated off time, it is necessary to compensate for that time error. The voltage charging time in the parasitic capacitance is indicated by the dotted line and is measured to be approximately 1.07 ms. The calculated \( T_{\text{comp}} \) is approximately 1.06 ms, which is close to the measured delay time.

Fig. 12 shows the dynamic response of the controller under load variation. It starts at full load and changes into half-load in 4.25 s. Fig. 10(c) shows the power estimates. The DC-link power is estimated by measuring the output of the inverter. At half-load, the switching frequency is changed from 31 kHz to 130 kHz.

**6. Experiment**

Experimental conditions are the same as the simulation conditions shown in Table 1. A digital signal processor TI DSP TMS320F28335 was used as the digital controller to realize the proposed method. An oscilloscope DPO 5104 and a power analyzer HIOKI 9340 were used for the measurement.

Fig. 13 shows a prototype of the experimental system. In order to verify the proposed strategy, the algorithm was implemented using a digital signal processor (TMS 320F28335). A single 32-bit floating-point DSP with a single-cycle execution time of 13.3 ns was used, and the switching period of the PWM is 100 µs. The prototype is composed of power supply, an AD converter, and a DSP, input filters, boost inductors, output filter, and the PFC/inverter. Silicon carbide powers MOSFETs (C2M0080120D) were used as switches for the inverter and PFC converter system.

Fig. 14 shows the experimental waveform when the time delay is not compensated. \( V_u \) represents the input voltage, \( I_{\text{boost1}} \) and \( I_{\text{boost2}} \) represents the current flowing to \( L_{\text{boost1}} \) and \( L_{\text{boost2}} \), respectively, and \( I_{\text{in}} \) represents the input current. Similar to the simulation in Fig. 9, current delay occurs near the zero point of the input current due to the time delay caused by resonance. Therefore, current distortion
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appears in $I_{in}$ and $I_{boost1,2}$.

Fig. 15 shows the experimental waveform when the time delay is compensated for. The experimental conditions are the same as those of the simulation in Fig. 10. Compared with Fig. 14, the input and inductor current waveforms were improved due to the time delay compensation. The THD of the input current is 4.3 %, power factor of the input voltage and current is 0.99 and efficiency is 97 %. The measurement results meet the standards such as EN 61000-3-2.

Fig. 16 shows the calculation results in the experiment of Fig. 15. $i_{pk_est}$ represents the peak value of the inductor current calculated using Eq. (3) and is identical to the $I_{boost1,2}$ in Fig. 15. $f_s$ represents the switching frequency and is shown to operate at approximately 15-80 kHz. $C_{comp}$ represents the proposed compensation time for the time delay.

Fig. 17 shows the time delay at the peak current. A time delay occurs during charging and discharging of $V_{d1}$ and $V_{d2}$. It is difficult to confirm the resonance in the waveform of current $I_{boost}$ due to parasitic components that are not taken into consideration, but time delay similar to simulation occurs.

Fig. 18 shows the Compensation time, time delay in simulation and time delay in experiment.

The inverter output voltage, DC-link voltage, and filter current compensation time and the delay time shown in the simulation are very similar. Since there is no consideration of other parasitic components, there is a slight error in the experiment and the simulation, but the influence of the parasitic component of the semiconductor device can be confirmed.

Fig. 19 shows the inverter experimental waveform. The inverter output voltage, DC-link voltage, and filter current are measured for the inverter control and PFC sensorless control.
Fig. 20. Dynamic response: Ch1 DC-link voltage, Ch2 input current, and Ch3 DC-link power estimate

Fig. 20 shows the dynamic response of the proposed controller under load variation. The experimental condition is changed from full load of 250 W to half load of 125 W, and after approximately 350 ms, it is transferred to full load again. The DC-link voltage $V_{dc}$ is well controlled to 380 V. $P_{dc,est}$ shows that the DC-link power is well estimated according to load variation.

7. Conclusion

CRM has excellent operating characteristics at low power. Although many sensorless techniques have been developed, further research on current sensorless control of CRM is needed. In this paper, a study was conducted to implement sensorless control under CRM. A current sensorless method that can be used in a PFC configured with an inverter has been proposed. In order to perform current sensorless, the input current must be estimated. However, due to the resonance between parasitic capacitance of the switch and the boost inductor, a time delay error occurs between the estimated inductor current and the actual value. Therefore, in this study, we also proposed a compensating scheme for time delay error caused by resonance. The compensation method was used to improve the current distortion in CRM. 250W prototype was fabricated. The THD of the input current is 4.3 %, power factor of the input voltage and current is 0.99 and efficiency is 97 % in experiments.

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