Through Silicon Stack (TSS) Assembly for Wide IO Memory to Logic Devices Integration and Its Signal Integrity Challenges

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Abstract

The current expanding mobile markets incessantly demands small form factor, low power consumption and high aggregate throughput for silicon-level integration such as memory to logic system. One of emerging solution for meeting this high market demand is 3D through silicon stacking (TSS) technology. Main challenges to bring 3D TSS technology to the volume production level are establishing a cost effective supply chain and building a reliable manufacturing processes. In addition, this technology inherently help increase number of IOs and shorten interconnect length. With those benefits, however, potential signal and power integrity risks are also elevated; increase in PDN inductance, channel loss on substrate, crosstalk and parasitic capacitance. This paper will report recent progress of wide IO memory to high count TSV logic device assembly development work. 28 nm node TSV test vehicles were fabricated by the foundry and assembled. Successful integration of memory wide IO chip with less than a millimeter package thickness form factor was achieved. For this successful integration, we discussed potential signal and power integrity challenges. This report demonstrated functional wide IO memory to 28 nm logic device assembly using 3D package architecture with such a thin form factor.

Ⅰ. Introduction

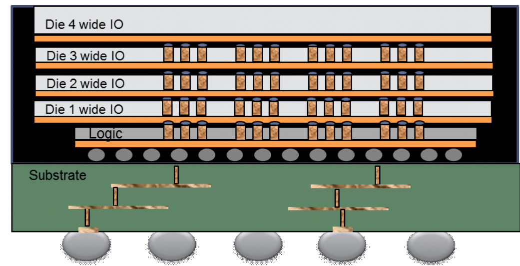
Significant works recently have been done to introduce through silicon via 3D package solutions to mobile platform such as smartphones and tablet devices where smaller form factor and superior performance are required to meet increasing demands for higher computing power and longer usage time [1], [2]. Traditional 3D package solutions like package on package (PoP), package in package (PiP), multi-die stack wire bond and 3D printing vertical interconnection etc. have been developed for more than a decade to provide small form factor as well as higher device package density. These package solutions might not be able to sufficiently deal with significantly increasing number of IOs to meet high data bandwidth requirement along with smaller form factor and low power needs for fast growing mobile market. It is because these traditional packages utilize only package peripheries to interconnect the multiple devices. In order to overcome the limitation of package solution as well as for the future scalability, a TSV structure with paring of wide IO memory integration technology, so called through silicon stack (TSS), has been developed.

Wide IO memory has higher IO counts (×512) than low power DDR memory (×32) which is mainly used for mobile application to enable higher data bandwidth

per operation frequency while power consumption can be lower due to its low operation frequency per data bit by parallel data processing. Samsung reported that the wide IO memory can lower memory active power up to 50 % [3]. Because of the wide IO memory's large number of pin counts which is normally more than 1,200 pins including proper power and ground with pad pitch of 40 um, conventional 3D package technologies described in early of this introduction could not offer enough interconnect density for logic die and wide IO memory integration. Also, possible long interconnect line of conventional 3D technologies could degrade wide IO memory's power advantage as well as enough form factor shrinkage. To overcome these issues and provide best integration form factor, TSS technology has been actively investigated.

To achieve the highest memory capacity and fastest data bandwidth with lowest power consumption, JEDEC standard micro pillar grid array (MPGA) attached on the backside of logic device through silicon vias (TSV) with micro-bumps to interconnect memory and logic device shown in [Fig. 1]. This direct stack method by using high density TSVs can also deliver best form factor not only for X, Y dimension also for Z height. Less than a millimeter thick form factor package was successful integrated with 4 die MPGA functional wide IO memory and logic device.

Even though this 4 die MPGA was successfully integrated, its electrical performance needs to be investigated from the perspective of PDN/signal integrity. The TSS topology naturally decreases interconnect length and dramatically increase number of IO. However high dense IO route can easily increase coupling among signals and parasitic capacitance. Substrate leakages can introduce high channel loss. Also, a TSV has relatively



[Fig. 1] Schematic diagram of logic and 4 die wide IO memory MPGA TSS package.

larger inductance than on-die metal lines and can cause power distribution network (PDN) noise.

In this paper, TSS assembly integration work and its impact on device characteristics will be discussed. For assembly process integration work, we will present high quality micro-bump joint with minimum 40 um pitch achieved by using 28 nm node TV and MPGAs. Metallurgical micro bump analysis and environmental reliability test results which exceeded reliability spec for the mobile applications will be also presented. For success of electrical performance, potential signal and power integrity risk for the proposed work will be discussed.

Ⅱ. Test Vehicles & Assembly Flows

To demonstrate assembly process yield and device functionality, daisy chain and functional wide IO memory with JEDEC standard 4 channel MPGA interface were fabricated and assembled to the logic die. There are 3 components in this package as shown in <Table 1>: logic die with high density via middle TSVs, wide IO memory MPGA and package substrate. 28 nm process node logic die has minimum 10:1 aspect ratio of high density TSVs was thinned down to sub 100 um thickness to demonstrate best possible Z-height reduction.

Conventional flip chip C4 bumps was used for logic

〈Table 1〉 Configuration of TSS test vehicle.

TV features	Description
Logic die (tier 1)	28 nm node
TSV	Min. aspect ratio of 10:1
Tier 1 interconnect	LF C4
Memory (tier 2)	1~4 die JEDEC wide IO
Tier 2 interconnect	Cu micro-pillar
Substrate	Laminate FCCSP

die to substrate interconnection while metallic based micro bump pad with minimum of 40 um pitch was plated on the backside of the die for wide IO MPGA interconnection. The multi-die wide IO MPGA was assembled by memory manufacturers with JEDEC wide IO interface which has 4 channels with total 1,200 IOs. Mono to maximum 4 die MPGA wide IO memory devices with lead micro-copper pillar with lead free solder cap bumps were attached to logic die by multiple possible assembly options. As shown in 〈Table 2〉, possibly 3 different chip stack options, wafer to wafer (W2W), die to wafer (D2W), die to substrate (D2S), were considered to target mass volume production scenario. Among these three options, D2S option was finally selected due to its relatively higher throughput and its ability to accommodate different memory die size.

〈Table 2〉 Assembly flow options.

Chip stack flow	Throughput	Die size mismatch	Die yield sensitivity	Note
W2W	High	Not allowed	High	
D2W	Low	Limited	Low	WLUF for high UPH
D2D or D2S	Med	Allowed	Low	

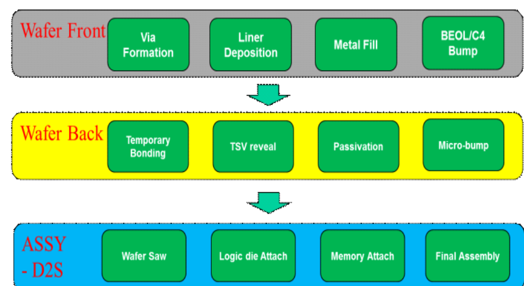
In D2S flow as shown in [Fig. 2], logic device wafer front and backside process was completed by foundry and then, fabricated TSV wafer shipped to assembly house with specially designed wafer-carrier to prevent the thin TSV wafers from any of shipping damage. Memory device was separately shipped from memory manufactures to assembly house for final assembly and test. Since logic die attach process is done before wide IO memory attachment, warpage optimization of logic die surface is very important to ensure high quality multi-tier interconnection integrity.

Ⅲ. Results and Discussion

3-1 Key Assembly Challenges and Mitigations

3-1-1 Wafer Handling and Shipping

As described in process flow session, fully processed thin wafer is supposed to be shipped from foundry to assembly house to enable D2S assembly flow. Shipping damage can cause die yield loss and more importantly liability issue since it is very difficult to address exact

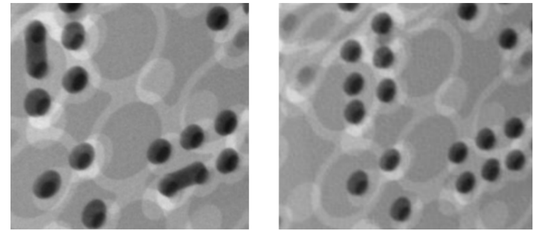


[Fig. 2] Schematic diagram of logic and wide IO memory MPGA TSS package assembly flow.

damage initiation point and failure reason of the damage in most of the cases. So, preventing shipping damage was achieved by using specially designed shipping carriers. This carrier can stack multiple wafers on the film frame and effectively reduced wafer damage incidents by suppressing wafer bending compared to conventional wafer cassette carrier.

3-1-2 Warpage Control

Warpage control of TSS package is one of the key challenge areas to achieve mass volume production level process yield and ensure wide enough process windows due to the tight pitch of wide IO memory and less than 100 um die thickness of logic die. Also, microbump of wide IO memory MPGA has less than 10 um thickness solder volume, maintaining flatness of the logic device after chip attach to the substrate is very important. Warpage of the package is very sensitive to the substrate strip design, bill of materials (BOM) and package materials selection, both assembly process conditions and material selections must be carefully optimized. After series of DOEs, optimized condition C were defined and showed more than 30 % warpage improvement over non optimized condition. Tilted X-ray images in [Fig. 3] showed that die corner bump bridge issue due to package warpage was successfully resolved by optimized condition C.



(a) Non optimized material and process condition A (b) Optimized condition C

[Fig. 3] Tilted X-ray image.

3-1-3 Memory MPGA Stacking

Due to the successful thin logic die chip attachment process optimizations, wide IO memory MPGA attachment process was developed. JEDEC standard wide IO memory interface requires microbump structures to accommodate minimum 40 um pitch IOs. Due to this tight pitch, 25 um diameter copper pillar with lead free solder cap microbump structure were used for memory to logic interconnection. To enable 40 um pitch bump with very thin solder compliant volume, thermal compression bonding (TCB) technique with pre-applied non-conductive paste was implemented. Unlike reflow bonding, TCB process achieves interconnection by individual die heating method. So, logic device on the substrate strip is not needed to heat up to the solder reflow temperature. Therefore, thin logic die warpage can be minimized while thin wide IO memory stack is also flatted by TCB vacuum head during TCB process. This unique feature of TCB process can deliver consistently excellent interconnection quality even with wide IO’s tight pitch and thin logic die structure.

3-1-4 Package Impact on Memory Characteristics

Dynamic random-access memory (DRAM) devices like wide IO memory store data in a capacitor (charge sensing device). So, stored data is very sensitive to thermal damage and discharge rate is exponentially increased by increasing operation temperature. To prevent data loss, periodical charge refresh is required for DRAM. This refresh rate is sensitive to the package assembly process and its stress so, it is a good indicator of package stress impact to the device. TSS package has multiple stack memory devices which are already gone

through memory manufacturer's packaging processes. So, assembly process to interconnect this multiple stack wide IO memory to the logic die adds another thermal and mechanical stress. To evaluate this impact, we characterized the total failure bit counts of memory cell as function of refresh time at 85℃. Failure bit counts increase by increasing refresh time as expected but first failure of each test unit is passed the 64 millisecond spec with big margin. This promising result confirms developed assembly process and material set for TSS package has low enough process impact to the memory device.

3-2 Potential PDN/Signal Integrity Challenges

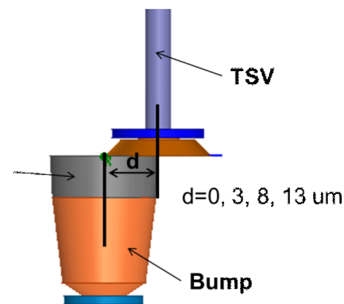
Memory interface for mobile platform requires stringent performance target as data rate increases. In order to ensure electrical performance in actual product with the proposed TSS technology, PDN/signal integrity needs to be considered carefully. In this paper, the proposed assembly method has been demonstrated by a proto type of test structure mainly for integration quality study and it is hard to extract practical level of PDN /signal integrity engineering judgment. Instead, this section generally discusses potential PDN/signal function risk with references and an example study.

3-2-1 Power Distribute Network (PDN)

Two or four die wide IO MPGA SS, which is demonstrated in this paper, is composed of a lot of numbers of signal and power TSVs. The inductance of TSV in general is higher than one-die metal traces. Thus, design of power and ground pairs is very important to reduce loop inductance to prevent PDN noise. TSV arrangement of powers and grounds is conducive to loop PDN loop inductance. [4], [5] discuss TSV arrangement modeling and design guidance for PDN inductance.

3-2-2 Signal Integrity

Along with power/ground TSVs for PDN performance, signal TSVs also needs to be carefully designed to fulfill its performance. First, A TSV structure forms a metal-oxide-semiconductor combination due to high aspect ratio of metal to embedded in silicon. Multiple stacking of TSVs can bring considerable parasitic capacitance, resulting in high latency of signal transmission. [6] describes technical guidance about TSV capacitance. Second, cross-talk in dense population of TSV array is of concern. Since a target application for the proposed structure demands high dense IO pin map with limited ground TSVs in stacked TSVs, cross-talk should be controlled to prevent a system fail due to near-end cross talk and far-end crosstalk. [7], [8] show crosstalk evaluation in 3D TSV. This is an example of study and case-by-case analysis should be considered with an assumed design space. In addition, high frequency-dependent loss from the silicon substrate and thin oxide-layer used in TSVs [9] and electrical performance degradation due to manufacturing variation may be taken into account in design stage to ensure the quality of the sig-



[Fig. 4] Picture of assembly misalignment scenario.

<Table 3> DC resistance variation.

d	0 um	3 um	8 um	13 um
DC R	21.4 mΩ	21.5 mΩ	22.3 mΩ	24.0 mΩ
Delta DCR	0 mΩ	0.1 mΩ	0.9 mΩ	2.6 mΩ
% DCR	0 %	0.5 %	4.0 %	12.0 %

nal propagation. For example, [Fig. 4] shows a study for DC resistance variation due to assembly misalignment between a TSV and a bump. The maximum misalignment (13 um) results in 12 % of DC resistance change as shown in <Table 3>.

Ⅳ. Summary

We presented TSS package development works and process optimization results and successfully demonstrated integration of up to 4 die wide IO memory MPGA on the logic die. Technical integration challenges of TSS package development and their mitigation were discussed along with memory characterization. Also, potential PDN/signal integrity risks were discusses with references and an example study. All of the data we presented in this paper inferred that there is no major road block to enable TSS technology for mobile products in terms of integration and electrical characteristics. However, we think introduction of this disruptive technology to the volume production will depend on not only technical progress but also business aspect of value propositioning.

References

[1] S. Q. Gu et al., "Stackable memory of 3D chip integration for mobile applications", *IEDM Tech. Dig.*, 2008.

[2] J. West, et al., "Practical implications of via-middle Cu TSV-induced stress in a 28 nm CMOS technology for wide-IO logic-memory interconnect", *Symposium on VLSI Technology*, art. no. 6242481, pp. 101-102, 2012.

[3] U. H. Kang et al., "8Gb 3D DDR DRAM using TSV technology", *IEEE Journal of Solid State Circuits*, vol. 45, no. 1, pp. 111-119, Jan. 2010.

[4] J. S. Pak, et al., "PDN impedance modeling and analysis of 3D TSV IC by using proposed P/G TSV array model based on separated P/G TSV and chip-PDN models", *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 208, 219, Feb. 2011.

[5] J. S. Pak, et al., "TSV mutual inductance effect on impedance of 3D stacked on-chip PDN with multi-TSV connections", *CPMT Symposium Japan, 2010 IEEE*, pp. 1, 4, 24-26 Aug. 2010.

[6] L. Zhang, et al., "Achieving Stable Through-Silicon Via (TSV) capacitance with oxide fixed charge", *Electron Device Letters, IEEE*, vol. 32, no. 5, pp. 668, 670, May 2011.

[7] Z. Xu, et al., "Crosstalk evaluation, suppression and modeling in 3D through-strata-via (TSV) network", *3D Systems Integration Conference (3DIC), 2010 IEEE International*, pp. 1, 8, 16-18 Nov. 2010.

[8] J. Cho, et al., "Modeling and analysis of Through-Silicon Via (TSV) noise coupling and suppression using a guard ring", *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 220, 233, Feb. 2011.

[9] H. Kim, et al., "Measurement and analysis of a high-speed TSV channel", *Components, Packaging and Manufacturing Technology, IEEE Transactions*

on, vol. 2, no. 10, pp. 1672, 1685, Oct. 2012.

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